Printed pages: 02 **Sub Code: MTCS201**

Paper Id: **210217** **Roll No:** | | | | | | | | | | |

M. TECH.
(SEM-II) THEORY EXAMINATION 2017-18
MULTICORE ARHITETURE AND PROGRAMMING

Time: 3 Hours ***Total Marks: 70***

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2 x 7 = 14

a. What are threads inside the OS and threads inside the Hardware?
b. What is Runtime Virtualization?
c. What is Task Decomposition and Data Decomposition?
d. What is Parallel Error Diffusion?
e. How Thread Synchronization takes place?
f. List few Open Library Functions?
g. Name some common Parallel Programming Problems?

SECTION B

2. Attempt any *three* of the following: 7 x 3 = 21

a. What are semaphores? What are its types? Explain with the help of an example.
b. Explain how Loop Scheduling and Portioning takes place.
c. Differentiate between Multi-core Architectures from Hyper- Threading Technology.
d. Explain Data Copy-in and Copy-out in detail.
e. What is Work-sharing Sections in parallel programming? Explain.

SECTION C

3. Attempt any *one* part of the following: 7 x 1 = 7

(a) Explain in detail about the synchronization primitives in parallel program challenges.
(b) What are Open MP directives? Explain data races and scalability in parallel program.

4. Attempt any *one* part of the following: 7 x 1 = 7

(a) Explain how threads are created and how they are managed.
(b) What is meant by Memory Consistency? How it can be achieved?

5. Attempt any *one* part of the following: 7 x 1 = 7

(a) Draw the architecture of Single core computer. Explain how it is different from multicore architecture.
(b) What are the problems with semaphores, locks, and condition variables? Explain in detail.

6. Attempt any *one* part of the following: 7 x 1 = 7

(a) Explain how Analysis of the Error Diffusion takes place? Write the algorithm involved.

(b) Write short note on shared memory programming with openMP.

7. Attempt any *one* part of the following: 7 x 1 = 7

(a) Explain how Thread Synchronization takes place, What are POSIX Threads?

(b) Explain the directory based cache coherence protocol to implement distributed shared memory architecture.