Printed Pages: 2 **Sub Code: RCAI202**

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MCA(INTEGATED)
(SEM II) THEORY EXAMINATION 2017-18
COMPUTER ORGANIZATION

Time: 3 Hours ***Total Marks: 70***

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2 x 7 = 14

a. What do you mean by register transfer language (RTL)?

b. The following transfer statement specifies a memory. Explain the memory operation

$$M[AR] \leftarrow R3$$

c. What do you mean by micro-operation?

d. Let the stack pointer SP=000000. How many items are there in the stack if : FULL=1 and EMPTY=0?

e. Convert the following arithmetic expression from infix to reverse polish notation

$$A + B * [C * D + E * (F + G)]$$

f. What do you mean by control bus?

g. Define cache memory.

SECTION B

2. Attempt any *three* of the following: 7 x 3 = 21

a. Construct the bus by using multiplexers.

b. Explain execution of complete instruction with example.

c. Write a program to evaluate the arithmetic statement X = (A + B) * (C + D) using 0, 1, 2 and 3 address instructions.

d. Explain the working of IOP in detail.

e. (a) How many 128X8 RAM chips are needed to provide a memory capacity of 2048 bytes?
(b) How many lines of address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?
(c) How many lines must be decoded for chip select? Specify the size of decoder.

SECTION C

3. Attempt any *one* part of the following: 7 x 1 = 7

(a) Design 4 bit arithmetic circuit and list out various micro-operations performed.

(b) Design a digital circuit that performs the four logic operations XOR, XNOR, NOR and NAND. Use two selection variables. Show the logic diagram of one typical stage.

4. Attempt any *one* part of the following: 7 x 1 = 7

(a) Discuss single bus organization with neat diagram.

(b) Write short note on hardwired control unit.

5. **Attempt any *one* part of the following:** **7 x 1 = 7**

(a) Explain register stack organization in detail.

(b) Discuss various types of addressing modes with examples.

6. **Attempt any *one* part of the following:** **7 x 1 = 7**

(a) Explain programmed I/O and interrupt driven I/O mode of transfer.

(b) Explain working of DMA transfer in detail.

7. **Attempt any *one* part of the following:** **7 x 1 = 7**

(a) Discuss various cache memory mapping techniques.

(b) Describe various page replacement algorithms with examples.