(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 214222 **Roll No.** | | | | | | | | | | |

MCA

(SEM. II) THEORY EXAMINATION 2013-14

COMPUTER ORGANIZATION

MCA215

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 214217 **Roll No.** | | | | | | | | | | |

(SEM. II) THEORY EXAMINATION 2013-14

COMPUTER ORGANIZATION

Time : 3 Hours *Total Marks : 100*

Note : Attempt **all** questions . Each question carries equal marks.

1. Attempt any **four** parts of the following : **(5×4=20)**

   (a) Discuss the advantages and disadvantages of polling and daisy-chaining bus arbitration schemes.

   (b) Draw the block diagram for the hardware that implements the following statements :

   (i) ab + cd : R ← AR +BR

   (ii) yz : R2 ← R1, R1 ← R2

   (c) Briefly explain high-speed adder ? Discuss design of high speed adders.

   (d) Discuss Micro-operations with suitable examples.

(e) Show the step by step process of Booth's multiplication with the help of flowchart and multiply :

(-13) and (-8) using Booth's algorithm.

2. Attempt any **four** parts of the following : **(5×4=20)**

(a) Explain the differences between hardwired control and micro- programmed control.

(b) Explain the process of fetching a word from memory and storing word in memory ?

(c) Discuss Multiple Bus Organization and its benefits.

(d) Discuss the step by step Execution of a complete instruction of Single Bus Organization

(e) Discuss Wide-Branch Addressing.

(f) List some common applications of micro -programming and explain them.

3. Attempt any **two** parts of the following : **(10×2=20)**

(a) Give the architecture of RISC and compare RISC with CISC Architecture.

(b) What do you mean by processor organization ? Discuss the advantages and disadvantages of :

(i) Single -accumulator based processor organization.

(ii) General- register based processor organization.

(iii) Stack based processor organization.

(c) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is :

(i) Direct

(ii) Immediate

(iii) Relative

(iv) Register Indirect

(v) Index with R1 as the index register.

4. Attempt any **two** parts of the following : **(10×2=20)**

(a) Briefly Explain DMA Controller ? Discuss the complete working of DMA with block diagram. Why does DMA have priority over the CPU when both request a memory transfer ?

(b) Write short notes on the following :

(i) I/O Interface

(ii) Interrupt and its types.

(c) Define Serial Communication. Briefly explain the role of protocols in communication

5. Attempt any **two** parts of the following : **(10×2=20)**

(a) Discuss the RAM chip design. A computer uses RAM chips of 1024×1 capacity.

(i) How many chips are need, and how should their address lines be connected to provide a memory capacity of 1024 bytes ×8 ?

(ii) How many chips are needed to provide a memory capacity of 16KB?

(b) Define Cache Memory. Explain its organizational structure. State why cache memory is always smaller than main memory.

(c) Briefly explain organization of 2D and 2½D memory and compare them.