Printed Pages :3

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NBC-204

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 194404

Roll No. | | | | | | | | | | |

M.C.A. (Dual Degree) (Semester-II)

SPL. THEORY EXAMINATION, 2014-15

COMPUTER ORGANIZATION

Time : 3 Hours] *[Total Marks : 100*

Note: Attempt all questions. Each question carry equal marks.

Q1 Attempt any four questions:

A. Explain Booth's algorithm for multiplication along with flow chart.

B. Design a 4-bit incrementer circuit using full adders.

C. Discuss various types of shift instructions.

D. Show the block diagram of one stage of arithmetic logic shift unit and explain its function table.

E. Discuss micro-operations with suitable examples.

F. Write short notes on register transfer.

Q2 Attempt any four questions:

A. Discuss multiple bus organization.

B. Discuss hardwired control unit.

C. Explain wide branch addressing with example.

D. How we can fetch the instruction from memory? Discuss.

E. Explain execution of complete instruction.

F. Explain the differences between micro-programmed and hardwired control unit.

Q3. Attempt any two questions:

A. Write a program to evaluate the arithmetic statement: X = A-B+C*D using one and three address instruction.

B. A bus organized CPU has 16 registers with 32 bits each, an ALU, and a destination decoder. How many multiplexers are there in A bus and what is the size of each multiplexer? How many inputs and out puts are there in the decoder.

C. Discuss RISC and CISC with their advantages and disadvantages.

Q4. Attempt any two questions:

A. Explain the working and actions of DMA with the help of a suitable diagram.

B. Describe CPU-IOP communication.

C. Explain Input/Output interface.

Q5. Attempt any two questions:

A. An address space is specified by 24 bits and corresponding memory space by 16-bits?

(i) How many words are there in the address space?

(ii) How many words are there in the memory space?

(iii) If a page consists of 2k words, how many pages and blocks are their in the system?

B. Compare direct and set-associative memory mapping in cache.

C. Discuss Virtual memory in detail.

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