Printed Pages : 3 MCA-215

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 7307 Roll No. | | | | | | | | | | |

M.C.A.

(SEMESTER-II) THEORY EXAMINATION, 2011-12

COMPUTER ORGANIZATION

Time : 3 Hours] *[Total Marks : 100*

Note : Attempt questions from **all** Sections as directed.

Section – A

1. Attempt **all** questions from this Section. $10 \times 2 = 20$

   (a) Draw the functional diagram of digital computer.

   (b) What is system bus ? Explain different types of buses.

   (c) What do you mean by micro-operation ? Explain.

   (d) What is the necessity of next address generation field ?

   (e) What is the difference between arithmetic shift and logical shift ?

   (f) Explain various fields of instruction format.

   (g) What is cache updating ? Why is it necessary ?

   (h) The application program in a computer system with cache uses 1400 instruction acquisition bus cycle from cache memory and 100 from main memory. What is the hit rate ?

   (i) Explain DMA idle and active cycles.

   (j) Give the major requirements for an I/O module.

Section – B

2. Attempt any **three** parts from this section. $3 \times 10 = 30$

   (a) Explain the hardware and algorithm for implementation of integer division.

   (b) Explain microprogrammed control unit and list advantage and disadvantage of microprogrammed control unit.

(c) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register RI contains the number 200. Evaluate the effective address if the addressing mode of instruction is

(i) Direct

(ii) Immediate

(iii) Relative

(iv) Register indirect

(v) Index with R_1 as the index register

(d) A computer employs RAM chip of 256 × 8 and ROM chips of 1024 × 8. The computer system needs 2 kbytes of RAM, 4 kbytes of ROM and four interface units, each with four register. A memory mapped configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM and 10 for interface registers.

(i) How many RAM and ROM chips are needed ?

(ii) Draw a memory address map for the system.

(iii) Give the address range in hexadecimal for RAM, ROM and interface.

(e) Classify and explain serial communication systems. Explain data communication formats in serial communication.

Section – C

3. Attempt **all** questions from this Section. **5 × 10 = 50**

Show the block diagram of one stage of arithmetic logic shift unit and also explain its functional table.

OR

Explain the modified Booth's algorithm. Perform multiplication for the following 6-bit numbers using Booth's algorithm.

Multiplicand 010111

Multiplier 110110

4. Explain the execution of a complete instruction with the help of example.

OR

Draw and explain typical hardwired control unit. Differentiate between hardwired and microprogrammed control unit.

5. Write a program to evaluate the arithmetic statement :

$E = (A + B) / (C + D) * F$

(a) Using a general register computer with three address instruction.

(b) Using a general register computer with two address instruction.

(c) Using a accumulator type computer with one address instruction.

(d) Using a stack organized computer with zero address operation instructions.

OR

Explain various data manipulation instructions and write a short note on RISC architecture.

6. What is an interrupt ? Explain how processor responds to an interrupt. What is the basic advantage of using interrupt – initiated data transfer over transfer under program control without an interrupt.

OR

Draw and explain the block diagram of 8089.

7. Define the terms address space and memory space. An address space is specified by 24 bits and corresponding memory space by 16 bits. Find the following :

(a) How many words are there in the address space ?

(b) How many words are there in the memory space ?

(c) If a page consists of 2K words, how many pages and blocks are there in the system ?

OR

What is cache memory ? Explain different cache mapping procedures with example.