(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 7307 Roll No. | | | | | | | | | | |

M. C. A.

(Second Semester) Theory Examination, 2010-11

COMPUTER ORGANIZATION

Time : 3 Hours] *[Total Marks : 100*

Note : This paper is in three Sections.

Section-A carries 20 marks.

Section-B carries 30 marks and,

Section-C carries 50 marks.

Section-A

You are required to answer ***all*** the parts. $2 \times 10 = 20$

1. Choose the correct answer for the following parts :

(a) Coprocessor .....

(i) is design to provide fast, low cast hardware implementation for complicated arithmetic function.

(ii) is a separate instruction-set processor that is closely coupled to the CPU.

(iii) is a processor whose instruction and registers are direct extensions of the CPU's.

(1) (i), (iii)

(2) (ii), (iii)

(3) (i), (iii)

(4) (i), (ii), (iii).

(b) Machine instructions are explicit commands that .....

(i) govern the transfer of information within a computer as well as between the computer and its I/O devices.

(ii) specify the arithmetic and logic operation to be performed :

(1) (i)

(2) (ii)

(3) both (i) and (ii)

(4) neither (i) nor (ii).

(c) In case of 2's complement representation expansion of bit length is ..... :

(1) Not possible

(2) Possible by adding additional bit position to the left and fill in with the value of the original sign bit.

(3) possibly by adding additional bit position to the right and fill in with the value of the original sign bit.

(4) Both (2) and (3).

(d) A coprocessor instruction typically contains which of the following fields ?

(i) an opcode

(ii) address

(iii) type of particular operation.

(1) (i), (iii)

(2) (i), (iii)

(3) (ii), (iii)

(4) (i), (ii), (iii)

(e) Which of the following is an advantage of microprogramming ?

(i) Microprogramming provides a well-structured control organization

(ii) A microprogramming control unit is more adaptable to changes :

(1) (i)

(2) (ii)

(3) both (i) and (ii)

(4) neither (i) nor (ii).

(f) A computer must have instructions capable of performing which of the following operations ?

(i) Data transfer between the memory and the processor register

(ii) Arithmetic and logic operations on data

(iii) Program sequencing and control

(iv) I/O transfers.

(1) (i), (ii)

(2) (ii), (iii), (iv)

(3) (i), (ii), (iii), (iv)

(4) (ii), (iv).

(g) While designing a control unit using hardwired control , a module-k sequence counter can behave like a cascade of .....delay elements :

(1) K

(2) K–1

(3) K+1

(4) K*K.

(h) Which of the following statement is correct about the advantage of register indirect addressing ?

(i) This mode is used to save progam space

(ii) This mode improve speed of program execution in some situation :

(1) (i)

(2) (ii)

(3) both (i) and (ii)

(4) neither (i) nor (ii).

(i) Which of the following statements is incorrect ?

(i) A horizontal microinstruction format allows no encoding of control information, whereas a vertical format does.

(ii) A vertical microinstruction can specify only one micro operation, while a horizontal microinstruction can specify micro operations.

(1) (i)

(2) (ii)

(3) (i) and (ii)

(4) neither (i) nor (ii).

(j) Which of the following is correct ?

(i) Memory access time is fixed, independent of the location of the word being accessed.

(ii) The small, fast RAM units called caches, tightly coupled with the processor and are often contained on the same integrated circuit chip to achieve performance.

(1) (i)

(2) (ii)

(3) both (i) and (ii)

(4) neither (i) nor (ii).

Section-B

Answer any ***three*** parts of the following : 10×3=30

2. (a) The outputs of four register $R0$, $R1$, $R2$, $R3$ are connected through 4-1 multiplexers to the inputs of the fifth register, $R5$. Each register is 8 bits long. The required transfer are dictated by four timing variables $T0$ through $T3$ as follows :

$T0 : R5 \leftarrow R0$

$T1 : R5 \leftarrow R1$

$T2 : R5 \leftarrow R2$

$T3 : R5 \leftarrow R3$

The timing variables are mutually exclusive which means that only one variable is equal to 1. At any given time, while the other three equal 0. Draw a block diagram showing the hardware implementation of register transfers. Includes the connection necessary from the four timing variables to the selection inputs of the multiplexers and to the load inputs of the register $R5$.

(b) Write a program to evaluate the arithmetic statement :

$$X = A - B + C*(D*E - F)/(G + H*I).$$

Using three, two, one and zero address instructions.

(c) Explain the Booth's algorithm for multiplication of signed 2's complement numbers along with flow chart and a suitable example.

(d) Design a variable length opcode to allow all of the following to be encoded in a 36-bit instruction :

(i) Instruction with two 15 bit addresses and one 3-bit register number.

(ii) Instruction with one 15 bit address and one 3-bit register number.

(iii) Instruction with no address or register.

(e) Explain the working and action of DMA interface with the help of block diagram and control signals, assuming suitable hardware configuration and instruction format.

Section-C

Note : ***All*** questions are compulsory. $10\times5=50$

3. Answer any two parts of the following :

(a) Discuss the 4-bit Carry Look-ahead Adder. Design the 16-bit Carry Look-ahead adder using four 4-bit Carry Look-ahead adders you have discussed.

(b) Express the following floating point number in IEEE 32-bit format.

$$-1.5\times10^{-20}$$

(c) Explain ISA, EISA bus Architectures.

4. Answer any two parts of the following :

(a) Let the address stored in the program counter be designated by the symbol $X1$. The instruction stored in $X1$ has an address part $X2$. The operand needed to execute the instruction is stored in the memory word with address $X3$. An index register contains the value $X4$. What is the relationship between these various quantities if the addressing mode of the instruction is (a) direct; (b) indirect; (c) relative; (d) indexed ?

(b) A bus-organized CPU has 16 register with 32 bits in each, an ALU, and a destination decoder.

(i) How many multiplexers are there in the A bus, and what is the size of each multiplexer ?

(ii) How many selection inputs are needed for MUX A and MUX B ?

(iii) How many inputs and outputs are there in the decoder ?

(iv) How many inputs and outputs are there in the ALU for data, including input and output carries ?

(v) Formulate a control word for the system assuming that the ALU has 35 operations.

(c) Write short notes on the following :

(i) Microinstruction

(ii) Micro program sequencer.

5. Answer any two parts of the following :

(a) Write the sequence of control steps required for the structure of single-bus organization for each of the following :

(i) Add the number num to register *r*1.

(ii) Add ((*R*2)), R1.

(b) Why are the read and write control lines in a DMA controller bidirectional ? Under what condition and for what purpose are they used as input ? Under what Condition and for what purpose are they used as output ?

(c) Discuss in brief with their advantages and disadvantage :

(i) RISC

(ii) CISC.

6. Answer any two part of the following :

(a) Desigen a Array multiplier that multiplies two 4-bit numbers. Use AND gates and binary adders.

(b) A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K * 32.

(i) Formulate all pertinent information required to construct the cache memory ?

(ii) What is the size of cache memory ?

(c) 16K×1 RAM chips are used to construct 64K×8 Memory.

How many chips will be required ? Draw a connection diagram ?

7. Answer any two part of the following :

(a) What is Cache Coherence ? How can the problems related to it be resolved ? Can this problem occur in Uniprocessor system ? Explain.

(b) Compare and contrast the direct and set associative mapping of cache.

(c) Explain 2D and 2½D Memory organization with block diagrams.