(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 7307 Roll No. | | | | | | | | | | |

M.C.A.

(SEM II) EVEN SEMESTER THEORY EXAMINATION, 2009-2010

COMPUTER ORGANIZATION

Time : 3 Hours *Total Marks : 100*

Note : *The question paper contains three sections,* ***Section-A****,* ***Section-B*** *and* ***Section-C*** *with the weightage of* ***20****,* ***30*** *and* ***50*** *marks respectively. Follow the instruction as given in each sections.*

SECTION-A

This section contains ***10*** *questions of multiple choice. Attempt* ***all*** *parts of this section.* **(10x2=20)**

1. (a) The BCD adder to add two decimal digits needs minimum of :

(i) 6 Full adders and 2 Half adders

(ii) 5 Full adders and 3 Half adders

(iii) 4 Full adders, 3 Half adders

(iv) none of the above statement is true

(b) A distance 4 code is essential to have :

(i) Single error correction or double error detection.

(ii) Single error correction and double error detection.

(iii) Double error detection and correction.

(iv) Both single and double error correction.

(c) In an n-bit single error correcting code with p number of information bits and q number of check bits :

(i) $q \leq log_2 n$ (ii) $2^q = n$;

(iii) $2^q < p + q$ (iv) none of the above is true

Attempt any two pa

(a) When a device

(d) In indirect index addressing mode using the index register having value X and address A, the effective operand address is :

(i) (X + A);

(ii) Content of memory location addressed by (X + A)

(iii) X + content of memory location addressed by A.

(iv) A + content of memory location addressed by X.

(v) none of the above is true.

(e) Program size is likely to be minimum with :

(i) expanding opcode

(ii) fixed length opcode

(iii) data dependent opcode

(iv) none of the above statements are valid

(f) A 16-bit two level carry look ahead adder with 4-bit CLA blocks has :

(i) 6 gate delay ; (ii) 10 gate delay ;

(iii) 12 gate delay ; (iv) 14 gate delay.

(g) An array multiplier using 4×2 multiplier cells employs following number of cells to multiply a pair of n-bit numbers.

(i) n^2 (ii) $n^2/4$ (iii) $n^2/8$ (iv) $n^2/12$

(h) A computer uses RAM chips of 1024×1 capacity. How many chips are needed to provide a memory capacity of 16 k bytes.

(i) 16 (ii) 128 (iii) 32 (iv) none of these

(i) Virtual memory consists of :

(i) Static RAM (ii) Dynamic RAM

(iii) Magnetic Memory (iv) None of these

(j) A group of bits that tell the computer to perform a specific operation is known as :

(i) Instruction code (ii) Micro-operation

(iii) Accumulator (iv) Register

SECTION - B

2. Attempt **any three** of the following : **(3x10=30)**

   (a) Design a 4-bit combinational circuit incrementer using four full adders circuits. Explain its working.

   (b) (i) Show the step-by-step multiplication using Booth's algorithm for the following multiplication :

   $(-11) \times (-8)$.

   (ii) Discuss Multiple-bus organization.

   (c) What do you understand by hardwired control unit ? Give various methods to design hardwired control unit. Describe one of the design methods for hardwired control unit with suitable diagrams.

   (d) What are the characteristics of a good instruction format ? Explain the types of instruction format.

   (e) What are the parameters of a typical Hierarchical Memory system ? Derive the average access time $\overline{T}$ formula of a n-level hierarchical system.

SECTION - C

Note : All questions are *compulsory* : **(2x5=10)**

3. Attempt **any two** parts of the following :

   (a) Explain characteristics of CISC and RISC architecture for Microprocessor.

   (b) Discuss the Microprogram sequences for a control memory with the help of block diagram.

   (c) What do you mean by wide-branch addressing ? Explain with example.

4. Attempt **any one** parts of the following : **(1x10=10)**

   (a) Assume a Main memory has 4 page frames and initially all page frames are empty. Consider the following stream of references :

   1, 2, 3, 4, 5, 1, 3, 6, 1, 2, 3, 4, 5, 6, 5

   Calculate the bit ratio if the replacement policy used is as follows :

   (i) FIFO (ii) LRU

   Comment on result of main memory has 5 page frames instead of 4.

   (b) Describe DMA with suitable block diagram. Why does DMA have priority over the CPU when both request a memory transfer ? Explain.

5. Attempt **any two** parts of the following : **(2x5=10)**

(a) When a device interrupt occurs, how does the processor determine which device issued the interrupt ?

(b) Discuss the working principle of I/O Processors (IOP).

(c) Represent following numbers in IEEE754 floating point format :

(i) -1.5 (ii) $1/16$

6. Attempt **any one** part of the following : **(1x10=10)**

(a) What do you understand by asynchronous transfer of data how is it achieved with the help of handshaking ?

(b) A hierarchical cache-MS memory has the following specifications :

(i) The cache takes 80 nsec to access the index field of each set and 10 nsec to access the tag field within a set;

(ii) MS access time of 500 nsec;

(iii) 80% of memory references are for reads and 20% for writes;

(iv) The bit ratio of 0.90 for read access and 0.80 for write access. Compute :

(A) Average access time for read;

(B) Average access time for both reads and writes for write through and write back schemes;

(C) The bit ratio for the system for write back schemes.

7. Attempt **any two** of the following : **(2x5=10)**

(a) Write a program to evaluate the arithmetic statement :

$$X = (A + B * C/D)/(E - F + G)$$

Using one and zero address instructions.

(b) An address field in an instruction contains decimal value 14. Where is the corresponding operand located for :

(i) immediate addressing ?

(ii) indirect addressing ?

(iii) indirect index addressing ?

(iv) register addressing ?

(v) register indirect addressing ?

(c) How many times does the CPU need to refer to memory when it fetches and executes an indirect address mode instruction if the instruction is :

(i) a computation requiring a single operand ?

(ii) a branch ?