Printed Pages : 4 **MCA – 206**

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 1471 Roll No.

M.C.A.

(SEM. II) EXAMINATION, 2008-09

COMPUTER ARCHITECTURE & MICROPROCESSOR

Time : 3 Hours] *[Total Marks : 100*

Note : (1) Attempt **all** questions.
(2) All questions carry **equal** marks.

1 Attempt any **two** parts of the following :

(a) Give various architectural classification schemes. Also discuss the Flynn's classification in detail.

(b) Distinguish among computer terminologies in each of the following groups :

(i) Parallel processing at job level, the interinstraction level, and the intrainstruction level.

(ii) Uniprocessor system versus multiprocesser systems.

(iii) Control flow computers versus data flow computers.

(c) Design a binary integer multiply pipeline with five stages. The first stage is for partial product generation. The last stage is a 36-bit carry lookahead adder. The middle three stages are made of 16 carry save address (CSA), of appropriate length.

(i) prepare a schematic design of the five stage multiply pipeline. All line widths and interstage connections must be shown.

(ii) Determine the maximal clock rate of the pipeline if the stage delays are $\tau_1 = \tau_2 = \tau_3 = \tau_4 = 90\ ns$, $\tau_5 = 45\ ns$ and the latch delay is 20 ns.

(iii) What is the maximal throughput of this pipeline in terms of the number of 36-bit results generated per second.

2 Attempt any **two** parts of the following :

(a) Discuss the various possible hazards between read and write operations in an instruction pipeline and state the mechanism to detect and avoid these hazards.

(b) The following overlayed reservation table corresponds to a two-function pipeline :

	t_0	t_1	t_2	t_3	
s_1	A	B	*	A	B
s_2		A		B	A
s_3	B		AB		

(i) List all the four cross forbidden lists of latencies and corresponding combined cross-collision matrices.

(ii) Draw the state diagram for the two functional pipeline.

(c) Describe the following terminologies associated with pipeline computers and vector processing :

(i) Grudy cycle

(ii) Pipeline throughput

(iii) Branch target Buffering

(iv) Register tagging

(v) Victorizer.

3 Attempt any **two** parts of the following :

(a) (i) Draw a 16-input omega network using 2*2 switches as building blocks.

(ii) Show the switch setting for routing a message from node 1011 to node 0101 and from node 0111 to node 1001 simultaneously. Does blocking exit in this case?

(iii) Determine how many permutations can be implemented in our pass through this omega network.

(iv) What is the maximum number of passes needed to implement any permutation through the network?

(b) Discuss the following terms associated with a multiprocessor system: loosely coupled multiprocessor and tightly coupled multiprocessor.

(c) Explain the following terms as applied to communication patterns in a message passing network:

(i) Channel traffic or network traffic

(ii) Network communication latencies

(iii) Network partitioning for multicasting communications.

4 Attempt any **two** parts of the following :

(a) Describe the deterministic scheduling models of processor management techniques used in multiprocessor system with a suitable diagram.

(b) If the following block of computations, a and b are two external inputs and Z is the final output. Two intermediate results are labelled x and y.

$x \leftarrow a*a;\ \ y \leftarrow b*b,\ \ z \leftarrow (x+y)/(x-y)$

(i) Draw a data flow graph for this code block, where *, +, - and / are arithmetic operators.

(ii) Show a template implementation of the data flow graph in (i).

(iii) Indicate the events that can be done in parallel in the execution of the above block of codes.

(c) Discuss the architectural features of Intel-8085 microprocessor. Also draw the functional block diagram.

5 Answer any **two** of the following :

(a) Define instruction. What are the various type of instruction used in Intel-8085 microprocessor? Explain with suitable example.

(b) A set of ten bytes is stored in memory starting with the address XX50H. Write a program to check each byte, and save the bytes that are higher than 60_{10} and lower than 100_{10} in memory location starting from XX60H.

Data (H): 6F, 28, 5A, 49, C7, 3F, 4B, 78, 64.

(c) Calculate the 16-bit count to be loaded in register DE to obtain the loop delay of two seconds in Loop 2. Assuming the system clock period is 0.33 μs

	MVI B, 14 H	7
Loop 2 :	LXI D, 16- bit	10
Loop 1 :	DCX D	6
	MOV A, D	4
	ORA E	4
	JNZ Loop 1	10/7
	DCR B	4
	JNZ Loop 2	10/7