



2 Attempt any **two** parts of the following : **10×2=20**

(a) Consider the following reservation table for a four-stage pipeline with a clock cycle  $\tau = 20$  ns.

	1	2	3	4	5	6
$S_1$	X					X
$S_2$		X		X		
$S_3$			X			
$S_4$				X	X	

- (i) Draw the state transition diagram for scheduling the pipeline.
  - (ii) Determine the MAL associated with the shortest greedy cycle.
  - (iii) Determine the pipeline throughput corresponding to the MAL and given  $\tau$ .
  - (iv) Determine the lower bound on the MAL for this pipeline. Have you obtained the optimal latency from the above state diagram ?
- (b)
- (i) Explain the different types of vector instructions for register-based pipelined vector machines.
  - (ii) Write down the advantages and disadvantages of SIMD array processors.
- (c) Explain the following in brief : (any **four**)
- (i) Effect of branching on pipeline throughput.
  - (ii) Internal data forwarding
  - (iii) Lower bound and upper bounds of minimal average latency.
  - (iv) Difference between dependency and hazard
  - (v) Instruction level parallelism

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3 Attempt any **two** parts of the following : **10×2=20**

- (a) (i) Show the difference between perfect shuffle and inverse perfect shuffle data routing function.
- (ii) Explain the SIMD matrix multiplication.
- (b) Differentiate between blocking, non-blocking and re-arrangeable networks. Draw the interconnection network for  $8 \times 8$  omega network.
- (c) (i) Draw a 16-node barrel shifter static connection network. What is its node degree and diameter ? Explain its data routing function.
- (ii) Describe the UMA, NUMA and COMA based multiprocessor systems.

4 Attempt any **two** parts of the following : **10×2=20**

- (a) In the following block of computations a, b and c are three external inputs and z is the final output :

$$z \in \frac{-b + \sqrt{b^2 - 4ac}}{2a}$$

- (i) Draw a data flow graph using \*, +, -, / and ^ (for square root) as arithmetic operators.
- (ii) Indicate the events that can be done in parallel.
- (b) (i) Describe the function of 8086 instruction queue. How does it speed up processing ?
- (ii) Explain the role of Segment Registers, Base Registers, Index Register and Pointer Registers in 8086 microprocessor.

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- (iii) Detail the functionality of instruction pointer in 8086.
- (c) (i) Explain various scheduling models for multiprocessor system.
- (ii) Classify and explain the dataflow computer organizations.
- (iii) List the various multiprocessor scheduling strategies. Write advantage and disadvantage of each.

5 Attempt any **four** parts of the following : **5×4=20**

- (a) Write down a program in 8085 assembly language to unpack a 8-bit BCD number available at 2000 H memory location. Store the unpacked numbers at 2001 H and 2002 H memory locations.
- (b) Write an 8085 assembly language program to generate a rawtooth waveform at the output port 80 H.
- (c) Explain the functions of ALE and  $\overline{IO/\overline{M}}$  signals of the 8085 microprocessor.
- (d) Explain various addressing modes available in 8085 assembly language.
- (e) Explain the role of stack in making calls to subroutine in 8085. Also give difference between a subroutine and an interrupt service routine.