(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 1153 Roll No. 1 3 0 3 2 1 4 0 0 1

MCA

(SEM. I) ODD SEMESTER THEORY EXAMINATION 2013-14

COMPUTER SYSTEM DESIGN

Time : 3 Hours *Total Marks : 100*

Note :– Attempt all questions from each Section as indicated.

SECTION–A

1. Attempt **all** parts : **(10×2=20)**

   (a) Determine by means of a truth table the validity of De Morgan's theorem for three variables : $(ABC)' = A' + B' + C'$.

   (b) Simplify $A'BC + AC$ using Boolean algebra.

   (c) How many flip flops will be complemented in a 10 bit binary counter to reach the next count after (i) 1001100111 (ii) 0011111111 ?

   (d) Specify memory operation for the statement R2 ← M[AR].

   (e) Let SP = 000000 in the stack. How many items are there in the stack if :

   (i) FULL = 1 and EMPTY = 0

   (ii) FULL = 0 and EMPTY = 1 ?

   (f) What is the transfer rate of an eight-track magnetic tape whose speed is 120 inches per second and whose density is 1600 bits per inch ?

(g) Write a short note on input devices.

(h) Explain bus arbitration.

(i) What is branch prediction ? Why is it used ?

(j) Explain the term *benchmarking*.

SECTION–B

2. Attempt any **three** parts : **(3×10=30)**

(a) Multiply (+15) and (+13) by Booth multiplication algorithms.

(b) Show the block diagram of the hardware that implements the following register transfer statements : yT2 : R2 ← R1, R1 ← R2.

(c) How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes ? What size of decoder is used for this construction ?

(d) Discuss various internal communication methodologies.

(e) How is LOOK different from SCAN ?

SECTION–C

3. Attempt any **five** parts : **(5×10=50)**

(a) Construct 4 × 1 multiplexer by using 2 × 1 multiplexers.

(b) Design a digital circuit that performs the four logic operations of exclusive-OR, exclusive-NOR, NOR and NAND.

(c) Write 0, 1, 2, 3 address instruction for the arithmetic statement :

$$X = (A - B + C*(D*E - F))/(G + H*K)$$

(d) A two-way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128 K × 32. (i) Formulate all pertinent information required to construct the cache memory; (ii) What is the size of cache memory ?

(e) Explain Graphics Processing Unit.

(f) What is disk prefetching ? What are its advantages and disadvantages ?

(g) How the programs are compiled in assembly ? Explain.