Printed Pages : 4   **CA-104**

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 1153   **Roll No.** ☐☐☐☐☐☐☐☐☐

M. C. A.

(Semester-I) Theory Examination, 2012-13

COMPUTER SYSTEM DESIGN

Time : 3 Hours]   *[Total Marks : 100*

Note : Attempt questions from all Sections as per instructions.

Section-A

Attempt *all* parts of this question.   2×10=20

1.   (a)   How does carry differ from overflow ?

      (b)   What is overflow and how can it be detected ?

      (c)   What is the basic element of a sequential circuit ?

      (d)   Construct a truth-table for the following :

$$xyz + x\overline{yz} + \overline{xyz}.$$

      (e)   Define the term 'Optimum-performace'.

      (f)   Define "Arithmetic Mean" and "Geometric Mean".

      (g)   Show three-bit one's complement representation and corresponding signed decimal number that it represents.

(h) Define static linking and dynamic linking.

(i) Define total execution time of the program.

(j) What is assembly language?

Section-B

Attempt any *three* parts of this question.   10×3=30

2. (a) Write 'Booth multiplication algorithm' and use 'Booth algorithm' to multiply 010011 by 011011.

   (b) Explain with example how an overlapping register window reduces Calls/Returns overhead.

   (c) (i) Draw the timing diagram of a ring counter.

      (ii) Design a PIPO, which is 4-bit buffer register with parallel in and parallel out.

   (d) What is Bus arbitration? Explain all the Bus arbitration schemes with neat sketches.

   (e) (i) Show the Manchester encoding for the bit sequence 110011101.

      (ii) A disk that has 16 sectors per track uses an interval factor of 1:4. What is the smallest number of revolutions of the disk required to read all of the sectors of track in sequence?

(2)

Section-C

Attempt *all* questions of this Section.   10×5=50

3.   Attempt any two parts :   5×2=10

(a)   Explain the four-stage instruction pipeline with neat block diagram.

(b)   Compare RISC architectures characteristics that distinguish them from CISC architectures.

(c)   List the capabilities of Commercial Assemblers.

4.   Attempt any two parts :   5×2=10

(a)   Draw and explain DMA flow-chart for a disk-transfer.

(b)   Explain Instruction Set Design issues with examples. Enumerate classes of instruction sets in a typical processor.

(c)   A bit mapped display is 1024 pixels wide by 1024 pixels high. The refresh rate is 60 Hz, which means that every pixel is rewritten to the screen 60 times a second. But only one pixel is written at anytime. What is the maximum time allowed to write a single pixel ?

5.   Attempt any two parts :   5×2=10

(a)   Explain a set-associative mapping scheme for a cache memory.

(b)   Design a four-word by eight-bit RAM using a four-word by four-bit RAM.

(c)   Explain how CAM works and lists its uses.

(3)

6. Attempt any one part : 10×1=10

   (a) Design a DATA-PATH for finding sum of '*n*' numbers.

   (b) Explain the differences between :

      (i) DATA BUSES & ADDRESS BUSES

      (ii) System Clocks & Bus Clocks

      (iii) Memory mapped I/O and instruction based I/O.

7. Attempt any one part : 10×1=10

   (a) Explain with examples different methods of representing floating point numbers.

   (b) Give truth table of a 'NAND' logic gate, with two inputs. Show diagrammatically how a 'OR' logic gate can be realized using only 'NAND' gates.

(4)   **5300**