Printed pages: 02 **Sub Code:RCA104**

Paper Id: **214104** **Roll No:** | | | | | | | | | | |

MCA

(SEM I) THEORY EXAMINATION 2018-19

COMPUTER ORGANIZATION & ARCHITECTURE

Time: 3 Hours ***Total Marks: 70***

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.
2. Any special paper specific instruction.

SECTION A

1. Attempt *all* questions in brief. 2 x 7 = 14

a. Convert the following.
   (i) $(1111101)_2 = (?)_{10}$
   (ii) $(425)_6 = (?)_4$
b. What is 2D and 2D1/2 memory organization? Explain using figure.
c. Define interrupt with its types.
d. Subtract using 2's compliment method
   (i) (-42) – (-13)
   (ii) (27) + (-41)
e. What is pipelining? Why do we need instruction pipelining?
f. Explain memory management hardware.
g. Simplify the Boolean expression using three variable map
   $F(A,B,C)=\sum(0,2,3,4,6)$

SECTION B

2. Attempt any *three* of the following: 7 x 3 = 21

a. What are the basic difference between a branch instruction, a call subroutine instruction and program interrupt also Explain micro program sequencer with block diagram
b. Explain how Booth's algorithms is suitable for signed number multiplication in comparison to conventional shift and add method using booth's multiplication multiply (-23) and (17).
c. Difference between isolated input/output and memory input/output? What are the advantages and disadvantages of each?
d. List out the advantages and limitation of hardwired control unit. Explain the organization of a microprogramed control unit.
e. Write a program to evaluate the arithmetic statement

$$X=\frac{A-B+C*(D*E-F)}{G+H*K}$$

   (i) Using general register computer with three address instruction.
   (ii) Using general register computer with two address instruction.
   (iii)Using general register computer with one address instruction.

SECTION C

3. Attempt any *one* part of the following: 7 x 1 = 7

(a) Explain IEEE standard for floating point representation.? Represent following in IEEE single precision and double precision format
a). 179.125810
b). 62350.4584

(b) Explain the bus arbitration in detail along with its types. What are different types of buses used?

4. Attempt any *one* part of the following: 7 x 1 = 7

(a) A computer has 16 registers, an ALU with 32 operations, and shifter with eight operations, all connected to a common bus system.
(i) Formulate a control word for a micro operation.
(ii) Specify the number of bits in each field of the control word and give a general encoding scheme.
(iii)Show the bits of control word that specify the micro – operation
a). R4← R5+R6
b). R2← R1 - R3

(b) A virtual memory system has an address space of 8k words, a memory space of 4k words and page and block/frame sizes of 1k words. The following page reference changes occur during time interval.
4 2 0 1 2 6 1 4 0 1 0 2 3 5 7
Determine the four pages that are resident in main memory after each page reference change if the replacement algorithm used is
(i) FIFO
(ii) LRU
(iii)OPTIMAL

5. Attempt any *one* part of the following: 7 x 1 = 7

(a) Explain Addressing modes along with their types. Design 4- bit bi-directional shift register.

(b) What is DMA? Explain DMA operation with diagramAlso Draw and explain the block diagram of typical DMA controller.

6. Attempt any *one* part of the following: 7 x 1 = 7

(a) (i)What is cache coherence? How can the problems related to it be solved?
(ii) How many **128x8** RAM chips are needed to provide the memory capacity of 2048 bytes? And how many lines must be decoded for chip select? And specify the size of the decoders.

(b) Discuss RISC and CISC architecture in detail. Also explain how data transfer can be controlled using hand shaking technique.

7. Attempt any *one* part of the following: 7 x 1 = 7

(a) Discuss Flynn's classification of various computer architecture with the help of theirfunctional block diagram.

(b) What is parallel processing and its various challenges? Explain any parallel processing mechanism.

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