Printed Pages:01 Sub Code: NIC-044

Paper Id: 1 3 2 8 1 4 Roll No.

B TECH

(SEM VIII) THEORY EXAMINATION 2017-18

DIGITAL SYSTEM DESIGN USING VHDL

Time: 3 Hours ***Total Marks: 100***

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2 x 10 = 20

a) What is Subprogram?
b) What are the reserve words in VHDL?
c) What is library?
d) Draw the Basic components of VHDL?
e) What is concurrent signal assignment and its use?
f) What is sequential wait statements?
g) What are the different modelling in VHDL?
h) What is the need of Delta Delay?
i) What is Von Neumann Computer Model?
j) What is design test?

SECTION B

2. Attempt any *three* of the following: 10 x 3 = 30

a) Discuss the different data types and operators in VHDL?
b) Discuss the Iterative networks and their component with detail description and symbol?
c) Use guarded signal assignments to describe a simple latch with q and NOT q outputs that function the same as a latch formed by cross-coupled NOR gates with clocked inputs. Use reasonable delay values?
d) Discuss the modelling a multiplexer with sequential statements?
e) Discuss the Huffman coding style for Finite State Machine with suitable diagram?

SECTION C

3. Attempt any *one* part of the following: 10 x 1 = 10

a) Discuss sequential modeling and attributes in VHDL?
b) Discuss array loops and assert statements in VHDL?

4. Attempt any *one* part of the following: 10 x 1 = 10

a) Discuss the basic structures of VHDL?
b) What are the standard packages used in VHDL? Discuss them?

5. Attempt any *one* part of the following: 10 x 1 = 10

a) Discuss about VHDL Library structure? How can create libraries and use them?
b) Discuss different TYPE-related issues in VHDL for hardware modeling?

6. Attempt any *one* part of the following: 10 x 1 = 10

a) Discuss the Inertial and transport delay Mechanism?
b) Discuss how multiple driving values are resolved to produce a value for a signal with multiple assignments?

7. Attempt any *one* part of the following: 10 x 1 = 10

a) Write the short note on any two-
   i. Array Multiplier
   ii. Carry-Look ahead Adder
   iii. Synthesizable Booth Multiplier
b) Describe Sequential Multiplier Design in detail?