

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 2752 Roll No.

--	--	--	--	--	--	--	--	--	--

B.Tech.

(SEM. VII) ODD SEMESTER THEORY

EXAMINATION 2012-13

DIGITAL MEASUREMENT TECHNIQUES

Time : 3 Hours

Total Marks : 100

Note :- Attempt **all** the questions. All questions carry equal marks.

1. Attempt any **four** parts : **(5×4=20)**
 - (a) Sketch and explain the waveform for a circuitry that is used for measurement of time interval between two events defined by V_L and V_H voltage levels.
 - (b) The periods of the main and the Vernier oscillators of a time interval meter are $10.005 \mu s$ and $10.000 \mu s$, respectively. (i) What is the resolution of the meter ? (ii) What is the maximum Vernier count ? (iii) If the reading on the main and the Vernier counters are both 1850, what is the time interval measurement ?
 - (c) A phase meters has the input signal $V_R(t) = 4 \times 10^{-3} \sin \omega t$ and $V_P(t) = 10 \times 10^{-3} \sin(\omega t + 30^\circ)$. Determine the error in phase measurement, if the threshold voltage of the two comparators is 2mV.
 - (d) Explain why the conventional method of frequency measurement is not suitable for very frequency measurement.

- (e) Explain the various techniques to measure small time interval between two events.
- (f) Explain Phase measurement techniques without frequency error.

2. Attempt any **four** parts : **(5×4=20)**

- (a) Explain the method for high frequency measurement.
- (b) Draw the circuit to display the peak frequency of input signal and explain it.
- (c) Discuss the measurement technique of low frequencies in a narrow band.
- (d) The clock frequency of a digital counter is 1MHz. Find the value of the unknown frequency f which is measured with the same precision in the period mode as well in the frequency mode with a gating time of 2 seconds.
- (e) Draw a circuit diagram for maximum/minimum counter reading recorder.
- (f) Calculate the counter reading for power system frequency deviation techniques and discuss the problem which may occur in these techniques.

3. Attempt any **two** parts : **(10×2=20)**

- (a) Describe the methods for measurement of capacitance at high frequency.
- (b) Write a short note on Programmable Biquads.

- (c) Explain in detail the Digital Programmable Gain Amplifier. Design a programmable gain amplifier for the gains 0, -1, -2, -3, -7, choosing $R_T = 24 \Omega$.

4. Attempt any **two** parts : **(10×2=20)**

- (a) Derive an expression for weighted resistor DACs. A 12 bit DAC produces a maximum output of 10V. If there is an error ΔV in the output voltage due to the drift in the component values, how large can ΔV be before the least significant bit would no longer be significant ?
- (b) Explain the block diagram and working of digital ohm meter.
- (c) (i) In a 6-bit successive approximation converter, if the full-scale value represents 1V and the unknown voltage $V_x = 55/64$ V, find the various V_n . Plot V_n versus n .
- (ii) In an 8 bit tracking ADC the clock frequency is 1MHz. Find the maximum time required for lock in the worst case.

5. Attempt any **two** parts : **(10×2=20)**

- (a) What is the difference between VTC and VFC ? Explain with the help of proper diagram. Give the detail of any single type of VTC.
- (b) Differentiate indirect and direct type ADC and explain any one technique of direct type ADC.
- (c) Design a 3 digit 1-V DVM based on the dual slope principle, for the following specification. Clock frequency 200 kHz, conversion rate 25 samples/s, auto-ranging arrangement for 1, 10, 100, 1000 V ranges, independent of 50 Hz hum present in the signal, $R_{in} = 10 M\Omega$.