Printed Pages: 04   **Sub Code: EEE402/ NEE402**
Paper Id: 120243   **Roll No.**

B TECH
(SEM IV) THEORY EXAMINATION 2017-18
Network Analysis and Synthesis

Time: 3 Hours   *Total Marks: 100*

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1.   **Attempt *all* questions in brief.**   **2 x 10 = 20**

a.   Write down the properties of a tree in the graph.

b.   If $Z_L=4+2j$, what should be the value of Z_{th} for maximum power transfer.

c.   Write down the limitation of Superposition Theorem.

d.   If a network contains B branches, and N nodes, then the number of mesh current equations should be_____.

e.   What are transients and why are they produced.

f.   Determine the time constant of series RL circuit in which a constant supply of 100V is connected across the series combination of resistance of 4K Ω and inductance of 0.01mH

g.   Define complex frequency.

h.   Define Driving point function.

i.   Write down the properties of Hurwitz polynomial.

j.   What are the limitations of Foster forms?

SECTION B

2.   **Attempt any *three* of the following:**   **10 x 3 = 30**

a.   (i) Find out the number of possible trees for the figure given below:
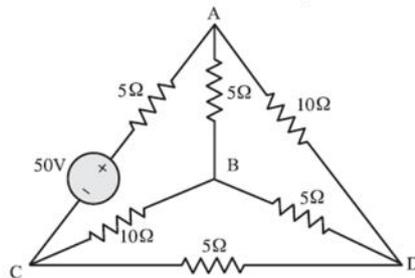
(ii) Obtain the oriented from the given Cut-set matrix:

$$[Q] = \begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 1 & 0 & 1 \end{bmatrix}$$

b.   Find the expression of the current i(t) in the circuit of figure 8 assuming that the switch is opened at t=0, the steady state having already reached before that.

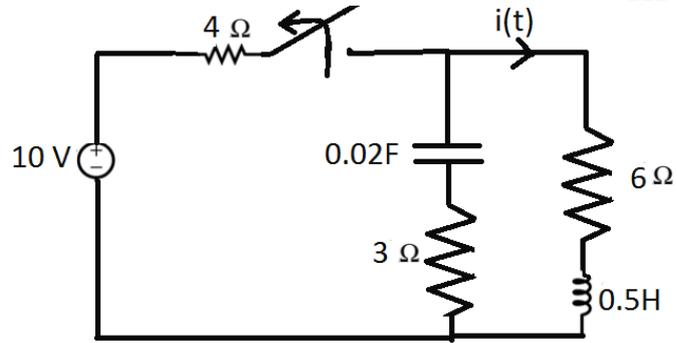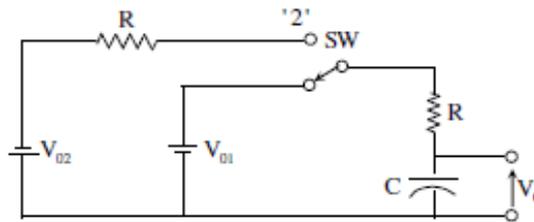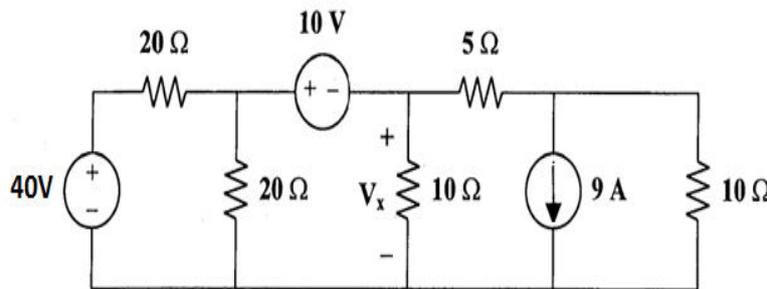**Figure 8**

c. The switch SW shown in the circuit is kept at position '1' for a long duration. At t = 0+, the switch is moved to position '2'. Assuming $V_{02} < V_{01}$, find the voltage $V_C(t)$ across capacitor in the figure given below:

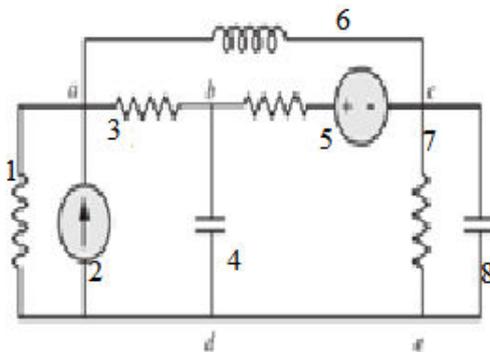d. Explain the concept of duality. Find the dual of the network shown in figure1.

e. Define Stermtest. Why it is used? Explain the process involved in Sterm test.

SECTION C

3. **Attempt any *one* part of the following:** **10 x 1 = 10**

(a) Write down the Cut-set and Tie-set matrix for the circuit given in fig. Consider 3, 5 and 4 as twigs. Also write down its Impedance Matrix.
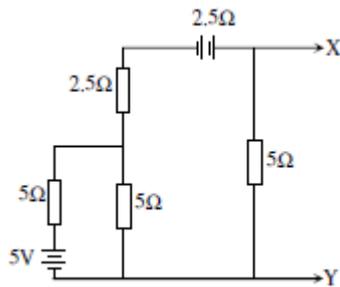

(b) For the network shown in the figure below, draw the oriented graph and create the tie-set matrix. Use this matrix to calculate current flowing through 5V source.
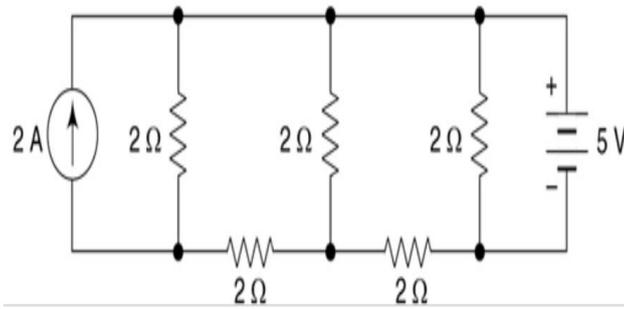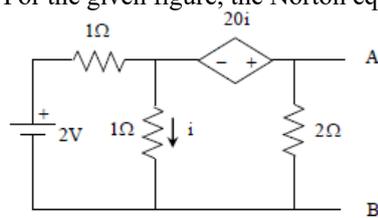
4. **Attempt any *one* part of the following:** **10 x 1 = 10**

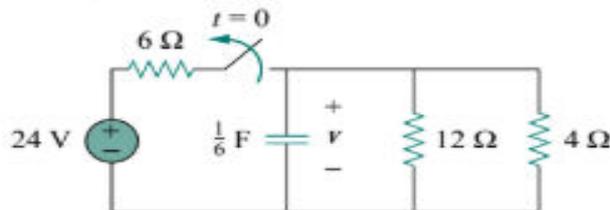(a) Obtain the Thevenin's equivalent circuit across the terminals X and Y in the ccircuit shown elow:

(b) For the given figure, the Norton equivalent circuit is to be determined across terminal AB.
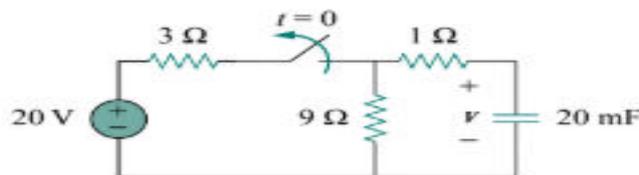

5. **Attempt any *one* part of the following:** **10 x 1 = 10**

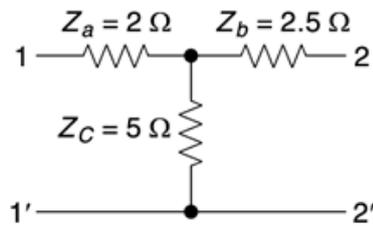(a) For the given circuit, find v(0+), dv(0+)/dt, $d^2v(0+)/dt^2$ & v(∞).

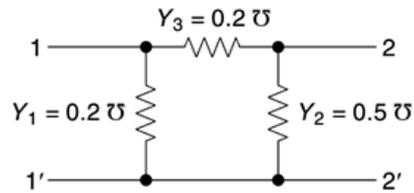(b) Find the expression for capacitive voltage for t>0 and initial energy which is stored in the capacitor.

6. **Attempt any *one* part of the following:** **10 x 1 = 10**

(a) Find the equivalent π-network for the *T*-network shown in the Fig.

(b) Find the equivalent T-network for the π-network shown in the Fig.

7. **Attempt any *one* part of the following:** 10 x 1 = 10

(a) How the function can be identified as a positive real function? Explain with a suitable example.

(b) Differentiate between Foster and Cauer forms and also write down the steps to obtain Foster-I and Foster-II forms.