(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0392 Roll No. | | | | | | | | | | |

B. Tech.

(SEM. VIII) THEORY EXAMINATION 2010-11

VLSI DESIGN

Time : 3 Hours *Total Marks : 100*

Note : (1) Attempt **all** questions. Assume the missing data if any.

(2) All questions carry equal marks.

1. Attempt any **four** parts of the following : **(5×4=20)**

(a) What are the factors that have led to the evolution and enhancement of VLSI ?

(b) What is the basic difference between diffusion and ion implantation processes ? Why ion-implantation is preferred in modern VLSI Design ?

(c) Sketch the cross section and explain the operation of n-channel enhancement type MOS transistor. Draw the characteristics of the device. How many diffusion steps are required to form it ?

(d) What is the self-aligned technique in MOS fabrication ? Discuss the problem associated with poly gate and suggest some method to avoid this problem.

(e) What are the different methods for CMOS fabrication ?

Explain any one of them in detail with suitable diagram.

(f) What are the advantages of low threshold voltage over high threshold voltage MOS devices ? Describe the various techniques to lower the magnitude of threshold voltage. How will you adjust the threshold voltage of a MOS device ?

2. Attempt any **two** parts of the following : **(10×2=20)**

(a) Draw and explain nMOS inverter with enhancement mode pull up and its transfer characteristics. Why depletion load is preferred compared to enhancement load.

(b) Construct a color coded stick diagram to represent the design of a CMOS circuit that implements the following function :

$$F = \overline{A} \bullet (\overline{B} + \overline{C})$$

(c) Discuss a combined voltage and dimension scaling model. Differentiate it with other scaling models. Compare the saaling factors for the following device parameters : Gate area, Gate Capacitance, channel resistance, current density, and power dissipation for the different scaling models.

3. Attempt any **two** parts of the following : **(10×2=20)**

(a) What is VLSI design rules ? Why is it required ? Describe the Lambda based design rules and layout methodology for CMOS circuit design. Explain with suitable diagram.

(b) What do you mean by sheet resistance ? Explain how the sheet resistance concept is applied to MOS transistor and inverters.

(c) Why is mask layout essential in VLSI design ? Construct the color coded stick diagram and mask layout for two input CMOS NOR gate.

4. Attempt any **two** parts of the following : **(10×2=20)**

(a) Describe the standard cell based design. Enlist the various standard cell library. What are the parameters of good VLSI design ?

(b) Draw six transistor SRAM cell and explain its different modes of operation.

(c) Draw and explain the generic FPGA architecture. Discuss the various programming technique emplyed in FPGA. Explain with suitable sketch.

5. Attempt any **two** parts of the following : **(10×2=20)**

(a) What is VLSI testing ? Explain different types of fault models used in VLSI testing.

(b) Discuss stuck at faults model. Explain a stuck at o/1 mode for testing a logic gate with suitable example.

(c) Discuss the following terminology :

(i) Exhaustive Testing

(ii) Structural Testing

(iii) Functional Testing.