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(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0392 Roll No.

B. Tech.

(SEM. VIII) EXAMINATION, 2008-09

VLSI DESIGN

Time : 3 Hours] *[Total Marks : 100*

Note : (1) Attempt all questions.
(2) Assume the missing data if any.
(3) All questions carry equal marks.

1 (a) Explain the following terms in brief (any **two** of the following) $2 \times 5 = 10$
(i) Self-aligned-process
(ii) MOS figure-of-merit
(iii) SALICIDE
(iv) Strong 0 or Strong 1
(v) Clocked CMOS.

(b) Of PMOS and NMOS transistor, which is better to obtain strong-I in a logic circuit? Give reasons in support of your answer. 10

2 Attempt any **two** parts of the following :

(a) If the gate oxide thickness in a SiO_2 based structure is 2nm, what would be the thickness of a HfO_2 (Dielectric constant k=20) based dielectric providing the same capacitance. 10
(Dielectric constant of SiO_2, $\varepsilon_r = 3.9$).

(b) In λ-based design rules discuss the thickness provided to n/p diffusion, Polysilicon layer, metal layer. How much should be the spacing between **two** layers of polysilicon or **two** layers of metal? **10**

(c) Why tubs or wells are used for the fabrication of n- or p-type MOSFETs? Why **two** tubs are used if the same transistor can be designed using single tub also? List the fabrication steps involved in twin-tub CMOS process. **10**

3 Differentiate between constant voltage scaling and constant field scaling. In both scaling techniques what effects are seen in the electrical performance of the device? **20**

OR

Discuss key features of Stick diagram. Implement a function "F" (given below) using CMOS gates and draw the stick diagram of this implementation. **20**

$$F = (A + B + C).\ (D.E)$$

4 If width of all the transistors are increased by α-times what will be the change in delay (τ) of the CMOS inverter circuit. Will the affect be same when instead of width the channel length is increased by the same factor a ? Why cascading is required for driving a large capacitive load? If a cascaded CMOS inverter is to drive a load of 2pF and its transistor has following parameters: **20**

$W_n = 7\ \mu$, $W_p = 10\ \mu$, $L_n = 1.5\ \mu$, $L_p = 1.5\ \mu$ and oxide thickness is 225A How many CMOS is required?

OR

4 Compare the pass-transistor logic circuit with that of transmission gates. **20**

(a) Implement 4 to 1 MUX circuit using CMOS transmission gates and explain its working.

(b) Explain the trade-offs between using a transmission gate or a tristate buffer to implement in FPGA routing block.

5 Attempt any **two** parts of the following : **10×2=20**

(a) Explain the difference between the tests you would use for logic verification or silicon debug and the tests you would use for manufacturing.

(b) Explain what is meant by a Struck-at-1 fault and a struck-at-0-fault.

(c) Explain the term controllability, observability and fault coverage.

(d) Explain how serial-scan testing is implemented.