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Printed Pages : 4 **TEC-042**

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0392 Roll No. ☐☐☐☐☐☐☐☐☐☐

B. Tech.

(SEM. VIII) EXAMINATION, 2007-08

VLSI DESIGN

Time : 3 Hours] *[Total Marks : 100*

Note : *(1) Attempt **all** questions.*

(2) Be precise in your answers.

(3) All questions carry equal marks.

1 Attempt any **four** parts of the following : **5×4=20**

(a) Discuss different steps involved in a typical n-well process.

(b) In how many ways tubs can be formed in a substrate ? Discuss the advantages associated with twin tub structure.

(c) What is the role of LOCOS technique in the development of VLSI circuits ?

(d) How does the non-uniform doping control the threshold voltage of MOS transistor ? Which other parameter can affect the threshold voltage effectively ?

(e) Obtain the transconductance (g_m) of an MOS transistor in terms of its circuit parameters.

(f) List the parameters that affect the switching speed of an MOS transistor. How does the figure of merit is related to the transconductance of an MOS transistor ?

2 Attempt any **four** parts of the following : **5×4=20**

(a) How does a $\beta-$ ratio shifts a VTC curve of an MOS based inverter circuit ? Give suitable reasons in support of your answer.

(b) Discuss the important features of Lambda based design rules.

(c) Determine the value of pull-up to pull-down ratio $\left(Z_{pu}/Z_{pd}\right)$ for an N-MOS inverter driven by another N-MOS inverter.

(d) If the pull-up to pull-down ratio is 4:1 in the above case and delay is $\tau = \mathbf{0.3}\,n$ sec across the first inverter determine the overall delay for the above pair.

(e) If a CMOS inverter charges and discharges through a capacitive load (C_L), obtain the expression for rise-time (t_r). (Assume $V_{tp} = 0.2\,V_{DD}$, where V_{DD} is the supply voltage). In order to achieve symmetrical operation of a CMOS inverter what design parameters are required ?

(f) If approximate value of R_S (ohms per square) of an n-channel transistor is $10^4\ \Omega/square$, calculate the channel resistance for the **Fig. 1** given below

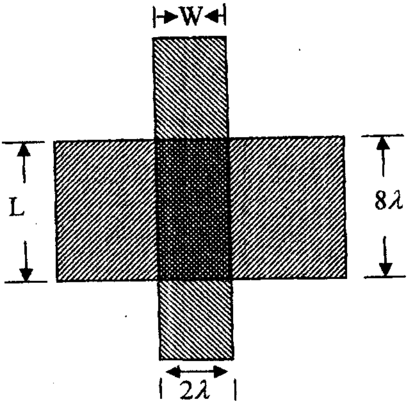

Fig. 1

3 Attempt any two parts of the following : **2×10=20**

(a) Discuss the scaling effect on MOS structures and limitation of scaling on the following on the following :

(1) Substrate doping

(2) Depletion width

(3) Limits of miniaturization

(b) Draw the color coded stick diagrams of two input n-MOS, CMOS, NAND and NOR gates.

(c) Consider a CMOS inverter circuit with the following parameters : $V_{DD} = 3.3\ V$,

$$k_n = 200\ \mu A/V^2,\ k_p = 80\ \mu A/V^2$$

$V_{T_{0,\,n}} = 0.6\,V$, $V_{T_{0,\,p}} = -0.7\,V$ and $k_R = 2.5$. Calculate the output voltage V_{out} and critical voltages $(V_{OL}, V_{OH}, V_{IL}\ and\ V_{IH})$ in the VTC and determine the noise margins of the circuit.

4 Attempt any **two** parts of the following : **2×10=20**

(a) What is FPGA ? Discuss the design flow of an FPGA chip. Mention certain advantages of it.

(b) With the help of a block diagram explain the sequence of steps to design an ASIC. Explain the term semi-custom and full-custom ASICs.

(c) Give the names of various ASIC design methodologies. Discuss in brief the LCA approach.

5 Write short notes on any **two** of the following : **2×10=20**

(a) Fault types of Models

(b) Controllability and Observability

(c) Built-in-self test (BIST) techniques

(d) Packaging technology
