Printed pages: 02 **Sub Code: EEC 034**

Paper Id: 131620 **Roll No:** | | | | | | | | | | |

B TECH
(SEM-VIII) THEORY EXAMINATION 2017-18
INTEGRATED CIRCUIT TECHNOLOGY

Time: 3 Hours ***Total Marks: 100***

Note: 1. Attempt all Sections.
2. Assume any missing data.

SECTION A

1. Attempt *all* questions in brief. 2 x10 = 20

a. What is Moore's law? Briefly describe the evolution of Ics.
b. Describe crystal defects that come in Silicon wafer.
c. Why Si3N4 is used for the isolation in CMOS IC fabrication?
d. Explain range of penetration in ion implantation.
e. What is the difference between Epitaxy and crystal growth?
f. What is etching? Explain the dry and wet etching.
g. What are the advantages of using poly silicon for the deposition of gate electrode?
h. Explain liquid source diffusion of Boron.
i. What are the applications of SiO_2 layer?
j. Show that to grow an oxide layer of thickness x, a thickness of 0.44x of silicon is consumed.

SECTION B

2. Attempt any *three* of the following: 10 x 3 = 30

a. What is epitaxial growth? Explain vapour phase epitaxy and also tell what are the sources of Silicon in vapour phase epitaxy.
b. What is ion beam lithography? Explain in detail.
c. Derive Flick's law of diffusion and explain different types of diffusion furnace with suitable diagram.
d. What is metalization? Describe the problems associated with this process.
e. Explain Monolithic and Itybrid Integrated Circuits.

SECTION C

3. Attempt any one parts of the following: 10 x 1 = 10

a. Discuss different steps in preparing wafers from raw Silicon.

b. Explain Electronic Grade Silicon with neat diagram. Explain the polishing process of Silicon in detail.

4. Attempt any one parts of the following: 10 x 1 = 10

a) Explain the kinetics of thermal oxidation. Why oxidation is done in CMOS technology?
b) How is the silicon nitrite used? Explain its deposition variables.

5. Attempt any one parts of the following: **10 x 1 = 10**

a) What is ion implantation? What are the advantages and disadvantages of this process over diffusion? Explain why annealing is required after ion implantation process

b) Define sheet resistance. Describe a method for its measurement. Estimate the number of gates that can be included on a logic gate array chip which is to be assembled in a 100 I/O package. Assume $\alpha = 4.5$ and $\beta = 0.5$.

6. Attempt any one parts of the following: **10 x 1 = 10**

a) Write a short note on package types and packaging design VLSI technology. What is meant by DIP? Explain in brief.

b) Write note on the following

(1) PVD process
(2) DC sputtering method for metalization.

7. Attempt any one parts of the following: **10 x 1 = 10**

a) Explain the n-MOS fabrication with suitable diagram.

b) Give the various fabrication steps of CMOS transistor using n- well technique with diagram and brief explanation.