Printed Pages:02 **Sub Code:NEC-042**

Paper Id: | 1 | 3 | 1 | 8 | 2 | 2 | **Roll No.** | | | | | | | | | | |

B TECH
(SEM-VIII) THEORY EXAMINATION 2017-18
DIGITAL SYSTEM DESIGN USING VHDL

Time: 3 Hours ***Total Marks: 100***

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

a. Differentiate the Signal and Variable.
b. Write the full form of IEEE.1164.
c. Listed the various data types of VHDL.
d. Write VHDL code for half Adder using style of modeling.
e. What is the Inertial delay?
f. Explain the sequential statement with respect to VHDL.
g. What are the Binding alternatives?
h. What do you mean by Test bench?
i. Explain the Guarded Signal Assignment.
j. Listed the applications of generics.

SECTION B

2. Attempt any *three* of the following: **10 x 3 = 30**

a. Implement D-flip-flop using structural style of modeling.
b. Differentiate between the conditional assignment statement and single statement with respect to 8:1 multiplexer.
c. (i) Explain the advantages and applications of VHDL.
(ii) Explain the importance of compilation and simulation in VHDL code.
d. Explain the design of Binary Multiplier with example.
e. Write the VHDL code and draw the SM chart for 486 bus interface unit.

SECTION C

3. Attempt any *one* part of the following: **10 x 1 = 10**

(a) What is the package body and package declaration? Explain with the suitable example.
(b) Write a VHDL code for 4-bit PIPO shift register.

4. Attempt any *one* part of the following: **10 x 1 = 10**

(a) Explain the coding format and different functions of UART.
(b) Explain the logic behind floating point Multiplication.

5. Attempt any *one* part of the following: 10 x 1 = 10

(a) What is Guarded signal assignment? Explain with suitable examples.
(b) What is the scan based design? Explain its testing sequence and general structure.

6. Attempt any *one* part of the following: 10 x 1 = 10

(a) What are the Multiple concurrent drivers? Explain different resolving methods.
(b) Explain the basic structure of Xilinx 4000 Series FPGA's.

7. Attempt any *one* part of the following: 10 x 1 = 10

(a) What do you mean by Testing? What are different issues related to design the test?
(b) Explain the various IEEE 754 floating point formats.