

B TECH
(SEM-VIII) THEORY EXAMINATION 2017-18
DIGITAL SYSTEM DESIGN USING VHDL

Time: 3 Hours

Total Marks: 100

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

- 1. Attempt all questions in brief. 2 x 10 = 20**
- a. Define the Packages and Library.
 - b. List the advantages of VHDL.
 - c. What do VHDL stands for?
 - d. Listed the various design flow of VHDL coding.
 - e. Write VHDL code for Half Subtractor using Behavioral style of modeling.
 - f. Listed the various VHDL operators.
 - g. Listed the applications of generics.
 - h. Write VHDL code for T flip-flop.
 - i. Write VHDL code 2: 1 Multiplexer.
 - j. What is the Delta Delay?

SECTION B

- 2. Attempt any three of the following: 10 x 3 = 30**
- a. What is the architecture declaration? Define its all types.
 - b. Write a VHDL description of a JK flip flop. Also explain the synthesis of VHDL codes.
 - c. Explain the file types and drivers.
 - d. Explain the design of Binary Divider with example.
 - e. Write the VHDL code for SRAM.

SECTION C

- 3. Attempt any one part of the following: 10 x 1 = 10**
- (a) Write the VHDL code for 4-bit decade counter.
 - (b) Write short notes on linked state machine.
- 4. Attempt any one part of the following: 10 x 1 = 10**
- (a) Explain the application and the use of status word register of UART transmitter.
 - (b) Write a short note on:
 - (i) CPLD
 - (ii) PLA

- 5. Attempt any *one* part of the following: **10 x 1 = 10****
- (a) Explain the SM chart transformation for microprogramming.
 - (b) (i) Give the syntax for wait and loop statements with suitable examples.
(ii) Discuss about the VHDL identifiers.
- 6. Attempt any *one* part of the following: **10 x 1 = 10****
- (a) Explain the basic structure of Xilinx 3000 Series FPGA's.
 - (b) Write a behavioral VHDL code for floating point adder using the IEEE single precision floating point format.
- 7. Attempt any *one* part of the following: **10 x 1 = 10****
- (a) Write and explain a state diagram for 101 sequence detector. Also write the VHDL code for the same.
 - (b) What do you understand from BIST techniques? Explain ORA and PRPG.