Printed Pages : 2

EEC032

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 131852

Roll No.

B. Tech.

(SEM. VIII) THEORY EXAMINATION, 2014-15

DIGITAL SYSTEM DESIGN USING VHDL

Time : **3** Hours] [Total Marks : **100**

Note: All questions are compulsory

1 Attempt **any four** parts: **5×4=20**

(i) Define Lexical elements, signals, variables and constant with reference to VHDL.

(ii) Explain compilation and simulation in VHDL code

(iii) Write structural VHDL description of 4-bit adder.

(iv) Write VHDL statement for Synchronous and Asynchronous D-Flip-flop.

(v) Explain Nine-Valued logic System for IEEE-1164 standard logic.

(vi) Differentiate between transport and Inertial delay model with examples.

2 Attempt **any two** parts: **10×2=20**

(i) Design the serial adder by accumulator with state diagram representation.

(ii) Design a behavioral model for 4x4 binary multiplier using state machine chart.

(iii) Write short notes on linked state machine.

3 Attempt **any two** parts: **10×2=20**

(i) Draw the state graph of Floating-point Multiplier with VHDL code using behavioral modelling.

(ii) Explain the logic behind floating point Multiplication.

(iii) Write short notes on XILINX-4000 FPGA.

4 Attempt **any two** parts: **10×2=20**

(i) Draw the block diagram of RAM with state machine diagram.

(ii) Draw the SM chart of Intel 486 bus interface and explain its bus cycle.

(iii) Write behavioural VHDL code for RAM.

5 Attempt **any two** parts: **10×2=20**

(i) Explain generic BIST scheme.

(ii) How fault can be detected using path sensitization method. Explain with example.

(iii) Explain Boundary Scan Testing.