(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 131852 Roll No. | | | | | | | | | | |

B.Tech.

(SEM. VIII) THEORY EXAMINATION 2013-14

DIGITAL SYSTEM DESIGN USING VHDL

Time : 3 Hours *Total Marks : 100*

Note :– Attempt **all** questions. All questions carry equal marks.

1. Attempt any **four** parts :

   (a) Differentiate between Combinational and Sequential Logic Circuits.

   (b) Write the applications and advantages of VHDL.

   (c) Write the syntax of declaration of an entity. Find error if any rectify the following :

   ```
   entity abc is
   port (x ; y : in std_logic;
         z, and : out std_logic);
         end abc
   ```

   (d) Write the operators in VHDL. Explain them in short.

   (e) Compare structural and behavioral style of modelling.

   (f) Compare variables and signals in VHDL.

2. Attempt any **four** parts :

(a) Write a VHDL code for full-adder using behavioural style of modelling.

(b) Write a VHDL code for 4:2 encoder with enable using structural style of modelling.

(c) Describe RTL design flow.

(d) What are different abstraction levels of a digital system design ?

(e) What are generic parameters ? Explain with examples.

(f) What are Binding Alternatives ?

3. Attempt any **two** parts :

(a) Write a VHDL code for 3:8 decoder.

(b) Write a VHDL code for 1:8 De-Mux.

(c) What is Guarded Signal Assignment ? Explain with example.

4. Attempt any **two** parts :

(a) Compare inertial delay mechanism and transport delay mechanism. Explain Delta Delay.

(b) What are Multiple concurrent drivers ? Explain different resolving methods.

(c) Write a positive EDGE triggered SR Flip Flop design in VHDL.

5. Attempt any **two** parts :

(a) Write a generic unconstrained n to 2^n decoder. Use std_logic. The decoder has an active low. Enable I/P, AN n BIT input and A 2^n output. The data inputs and the outputs are active high. When initiated, this decoder expands to its required size.

(b) Write a Push-Pop stack model using the VHDL access type. Push is done after a clock pulse, and pop is done first and then clocked. Use the access type so that the stack can be made with no limit. Data on the stack is a record of an 8-bit bit_vector and a time field. The stack has a clock input, but you will only be mimicking the clocking since the access type does not require a clock.

(c) What do you mean by testing ? What are different issues related to design test ?