

Printed Pages—2

EEC032

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 2887

Roll No.

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B. Tech.

(SEM. VIII) THEORY EXAMINATION 2011–12

DIGITAL SYSTEM DESIGN USING VHDL*Time : 3 Hours**Total Marks : 100***Note :-** Attempt all questions. Each question carries equal marks.1. Attempt any **three** parts of the following :- (20)

- (a) Define following in context with VHDL :
- (i) Structures
 - (ii) Objects
 - (iii) Data type.
- (b) Explain sequential statements and process by taking suitable examples.
- (c) Discuss sequential modeling and attributes.
- (d) Explain conditional assignment with the help of an example.
- (e) Explain array loops and assert statements by considering proper example.

2. Attempt any **three** parts of the following : (20)

- (a) Discuss basic structure of VHDL.
- (b) Write a VHDL module that describes a 16-bit serial-in, serial-out shift register with input S/ (serial input), EN (Enable) and CK (clock, shift on rising edge) and SO (serial output).

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- (c) Write a VHDL description of a SR latch.
 - (i) Use a combinational assignment statement
 - (ii) Use the characteristic equation
 - (iii) Use two logic gates
 - (d) Write a VHDL code for full subtracter using logic equations.
 - (e) Explain binding alternatives and genetic parameters.
3. Attempt any **three** parts of the following : (20)
- (a) Explain concurrent signal assignment with suitable block diagram and VHDL codes.
 - (b) Discuss guarded signal assignment with suitable VHDL codes.
 - (c) Explain different sequential statements with suitable block diagram.
 - (d) Explain declaration for initializing multidimensional arrays, non integer indexing and unconstrained arrays.
 - (e) Write the instructions used for :
 - (i) Opening and closing files
 - (ii) File read and write operation.
4. Attempt any **two** parts of the following : (20)
- (a) Explain inertial and transport delay mechanism with their comparison.
 - (b) Explain concurrent assignments and sequential placement of transactions.
 - (c) Explain delta delay and transaction appending rules.
5. Attempt any **two** parts of the following : (20)
- (a) Discuss issues related to core design test.
 - (b) Discuss synthesis rules and styles for hardware cores and models.
 - (c) Explain memory and queue structure. Also, discuss about arithmetic cores.