PAPER ID-410459

Roll No:

B.TECH.
(SEM VII) THEORY EXAMINATION 2021-22
VLSI Design

Time: 3 Hours   *Total Marks: 70*

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. **Attempt *all* questions in brief.**   **2 x 7 = 14**
   a. Give classification of IC packages
   b. What is channel length modulation
   c. Implement 2:1 MUX using CMOS Transmission Gate
   d. Give the circuit arrangement for 2 input NAND gate using CMOS logic
   e. Define interconnection
   f. Write the expression of dynamic power dissipation for MOS circuit
   g. Distinguish functionality test and manufacturing test

SECTION B

2. **Attempt any *three* of the following:**   **7x3= 21**
   a. Describe VLSI design strategies concepts of regularity, modularity and locality
   b. Write short note on: (i) Logical Effort (ii) Parasitic Delay
   c. Enlist the advantages of dynamic logic circuit over static logic circuit. Explain NORA CMOS logic circuit with suitable example
   d. What are the sources of power dissipation in CMOS circuits. Describe leakage power dissipation and dynamic power dissipation
   e. Why transistor scaling is of great importance in VLSI. Write down comparison between Constant field scaling and Constant voltage scaling

SECTION C

3. **Attempt any *one* part of the following:**   **7x1= 7**
   a. Discuss the hierarchy of various semiconductors with Moore's law. Draw the Y- chart and explain the VLSI design process
   b. Illuminate the n-well CMOS fabrication process with neat diagrams

4. **Attempt any *one* part of the following:**   **7x1= 7**
   a. Explain the Elmore Delay Model with suitable diagram
   b. Draw and explain the working of CMOS inverter with its transfer characteristics.

5. **Attempt any *one* part of the following:**   **7x1= 7**
   a. Draw and explain the working of Lumped RC-model for interconnects
   b. Explain the concept of voltage bootstrapping with the help of circuit arrangement

6. **Attempt any *one* part of the following:**   **7x1= 7**
   a. Explain the variable threshold CMOS circuits
   b. Draw the circuit diagram of SRAM and explain read and write operation

7. **Attempt any *one* part of the following:**   **7x1= 7**
   a. Explain the following:
      (i) Ad Hoc testable design techniques   (ii) Fault types and models
   b. Write a short note on Built-in-self test (BIST) techniques