Sub Code:NEC703

Paper Id: 130718 Roll No: | | | | | | | | | | | | | |

**B. TECH.**
**(SEM-VII) THEORY EXAMINATION 2019-20**
**VLSI DESIGN**

*Time: 3 Hours* *Total Marks: 100*

**Note:** Attempt all Sections. If require any missing data; then choose suitably.

**SECTION A**

**1. Attempt *all* questions in brief. 2 x 10 = 20**

a) Define LSI, MSI, VLSI, and ULSI on number of transistor basis.
b) Write down the Applications of FPGA.
c) What is sub threshold leakage current?
d) What is crosstalk delay in VLSI?
e) What is body effect?
f) Implement 2:1 MUX using CMOS Transmission Gate.
g) Write the Expression of dynamic power dissipation for MOS circuit.
h) Give the circuit arrangement for 2 input NAND gate using CMOS logic.
i) Define interconnection.
j) Why scaling has a great importance in VLSI circuits.

**SECTION B**

**2. Attempt any *three* of the following: 10x3=30**

(a). What are various processes of CMOS fabrication? Explain Twin tub processes with suitable sketch
(b). Derive the expression for $V_{IH}$, $V_{IL}$, $NM_L$, and $NM_H$ for CMOS inverter.
(c). Derive the equation for calculation of delay in multistage logic Network in terms of path effort and parasitic delay. What are the criteria for choosing best number of stages in it?
(d). Why transistor scaling is of great importance in VLSI. Write down comparison between Constant field scaling and Constant voltage scaling.
(e). Explain CMOS Domino circuit along with its features. How it can be cascaded in VLSI circuits.

**SECTION C**

**3. Attempt any *one* part of the following: 10x1=10**
(a) Draw the Y-chart and explain the concept of Design Hierarchy with the help of example.
(b) Explain the various strategies of VLSI system design.

**4. Attempt any *one* part of the following: 10x1=10**
(a) What are the sources of power dissipation in CMOS circuits? Explain Dynamic and static power consumption.
(b) What are interconnecting models? Explain any two of them in brief.

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**5. Attempt any *one* part of the following: 10x1=10**

(a) Write the Difference between Dynamic CMOS logic circuit and Static CMOS logic circuit. Explain the classification of Dynamic CMOS logic circuit and design a 2 input EXOR logic Gate using Domino logic.

(b) Explain the concept of voltage bootstrapping with the help of circuit arrangement.

**6. Attempt any *one* part of the following: 10x1=10**

(a) Explain the variable threshold CMOS circuits

(b) Draw the circuit diagram of SRAM and explain read and write operation.

**7. Attempt any *one* part of the following: 10x1=10**

(a) What are the different scan based techniques explain built in self-test technique.

(b) Explain the following:

(i) Ad Hoc testable design techniques (ii) Fault types and models.