PAPER ID-310756

Roll No: | | | | | | | |

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Subject Code: KEC072

BTECH
(SEM VII) THEORY EXAMINATION 2023-24
VLSI DESIGN

TIME: 3 HRS **M.MARKS: 100**

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief.

Q no.	Question	Marks	CO
a.	Why we need a low power VLSI circuit in today's scenario?	2	1
b.	Define LSI, MSI, VLSI, and ULSI on number of transistor basis.	2	1
c.	What is parasitic delay?	2	2
d.	Define logical effort with example.	2	2
e.	Differentiate between static power and dynamic power.	2	3
f.	What are the problems in single-phase clocking?	2	3
g.	Distinguish between SRAM and DRAM.	2	4
h.	Enlist the advantages of using address multiplexing scheme in DRAM cell.	2	4
i.	Explain the term controllability.	2	5
j.	Define the terms- Defects, Errors	2	5

SECTION B

2. Attempt any *three* of the following:

a.	Implement the CMOS logic for the following Boolean expression: (i) Y= (A+B+C).D (ii) Y= (A+B+C)(D+E).F (iii) 3 input NOR gate	10	1
b.	Explain the Elmore Delay Model with suitable diagram.	10	2
c.	Enlist the advantages of dynamic logic circuit over static logic circuit. Explain NORA CMOS logic circuit with suitable example.	10	3
d.	Explain the various types of power dissipation in CMOS circuits.	10	4
e.	What are the different scan based techniques explain built in self-test technique.	10	5

SECTION C

3. Attempt any *one* part of the following:

a.	What is need of VLSI Testing? Discuss about Functional and manufacturing tests.	10	1
b.	What are various processes of CMOS fabrication? Explain Twin tub processes with suitable sketch	10	1

4. Attempt any *one* part of the following:

a.	Draw and explain the working of Lumped RC-model for interconnects	10	2
b.	Write short note on: (i) Logical Effort (ii) Parasitic Delay	10	2

5. Attempt any *one* part of the following:

a.	Explain CMOS Domino circuit along with its features. How it can be cascaded in VLSI circuits.	10	3
b.	Explain the term Voltage Boot Strapping in CMOS logic with suitable examples.	10	3

6. Attempt any *one* part of the following:

a.	Write short note on DRAM cell. Explain leakage and refresh operation in DRAM cells	10	4
b.	Draw the circuit diagram of SRAM and explain read and write operation.	10	4

7. Attempt any *one* part of the following:

a.	Explain the following: (i) Ad Hoc testable design techniques. (ii) Fault types and models.	10	5
b.	Explain Adiabatic Logic Circuits	10	5