

B. TECH.
(SEM-VII) THEORY EXAMINATION 2019-20
VLSI DESIGN

Time: 3 Hours

Total Marks: 100

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A**1. Attempt all questions in brief.****2 x 10 = 20**

- a) Define LSI, MSI, VLSI, and ULSI on number of transistor basis.
- b) What are the advantages of Surface mount technology?
- c) What are the classifications of IC packages?
- d) What is use of stick diagram?
- e) Give the circuit arrangement for 2 input NAND gate using CMOS logic.
- f) What is parasitic delay?
- g) What is body effect?
- h) Implement 2:1 MUX using CMOS Transmission Gate.
- i) Write the Expression of dynamic power dissipation for MOS circuit.
- j) What is logical effort?

SECTION B**2. Attempt any three of the following:****10x3=30**

- (a) Explain the Fabrication Process of N-MOS transistor. Explain the MOSFET capacitance with suitable sketch.
- (b) (i) Describe the standard cell based design.
(ii) Consider a CMOS inverter with the following parameter $V_{DD}=3.3\text{ V}$, $V_{tn}=0.6\text{ V}$, $V_{tp}=-0.7\text{ V}$, $K_n=200\mu\text{A/V}^2$ and $K_p=80\text{ mA/V}^2$. Calculate the noise margin of the circuit.
- (c) Explain Domino and NORA CMOS logic circuit with suitable example.
- (d) Write short note on DRAM cell. Explain leakage and refresh operation in DRAM cells.
- (e) Explain the following:
 - (i) Scan Based Technique.
 - (ii) Fault types and models.

SECTION C**3. Attempt any one part of the following:****10x1=10**

- (a) Discuss the hierarchy of various semiconductors with Moore's law. Draw the Y- chart and explain the VLSI design process. <https://www.aktuonline.com>
- (b) What do you mean by Z_{pd} , Z_{pl} in the inverter circuit? Derive the required ratio between Z_{pd} and Z_{pl} of MOS inverter.

4. Attempt any one part of the following:**10x1=10**

- (a) Write short note on:
 - (i) Constant voltage scaling on delay
 - (ii) Power delay product
- (b) Briefly explain variable threshold CMOS (VTCMOS) circuit.

5. Attempt any one part of the following:**10x1=10**

- (a) Explain the different kinds of physical defect (faults) that can occur on a CMOS circuit.
- (b) Derive the expression for V_{IH} , V_{IL} , NM_L , and NM_H for CMOS inverter.

6. Attempt any one part of the following:**10x1=10**

- (a) Write the Difference between Dynamic CMOS logic circuit and Static CMOS logic circuit. Explain the classification of Dynamic CMOS logic circuit and design a 2 input EXOR logic Gate using Domino logic.
- (b) Explain the behavior of pass transistor in dynamic CMOS logic implementation. With a neat schematic diagram, explain SR flip flop implementation using pass transistor logic.

7. Attempt any one part of the following:**10x1=10**

- (a) Write a short note on Built-in-self test (BIST) techniques.
- (b) Explain various types of power dissipation in CMOS circuits.