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B.TECH
(SEM. VII) THEORY EXAMINATION 2017-18
VLSI DESIGN

Time: 3 Hours ***Total Marks: 100***

Note: 1. Attempt all Sections.
2. Assume any missing data.

SECTION A

1. Attempt *all* questions in brief. **2 x10 = 20**

a. Why we need a low power VLSI circuits in today's scenario?
b. Write short notes on controllability and observability.
c. How the latch up problem can be overcome?
d. Define Interconnect scaling.
e. Define the terms Defects, Errors and Faults.
f. Why we prefer CMOS transmission gates over other gates?
g. Define logical effort with example.
h. What are the various ways to reduce the delay time of a CMOS inverter?
i. What is meant by Stuck-at-1 (s-a-1) fault and stuck-at-0 (s-a-0) fault?
j. Draw the stick diagram of EXOR gate.

SECTION B

2. Attempt any *three* of the following: **10 x 3 = 30**

a. Draw the Y-Chart and explain the VLSI design process.
b. Enlist the layout design process and design rules of CMOS circuit. Draw a stick diagram of CMOS NOR gate.
c. Explain two input XOR gate using CMOS logic circuits, TG gate and Pass Transistor logic.
d. Consider a CMOS inverter circuit with the following parameters: V_{DD} = 5V,$V_{TO,n}$ = 0.8V , $V_{TO,p}$ = -0.1V , $\mu_n C_{ox}$ = 50uA/v^2 , $\mu_p C_{ox}$ = 20uA/v^2 , λ=0. Both transistor have a channel length of $L_n = L_P$ =1um, the total output load capacitance of this circuit is C_{out} = 2pF.which is independent of transistor dimensions.
i) Determine the channel width of the nMOS and pMOS transistors such that the switching threshold voltage is equal to 2.2V and the output rise time is τ_{rise} = 5ns.
ii) Calculate the average propagation delay time τ_p
e. Discuss the operation of CMOS SRAM cell circuit. Also describe in brief Adiabatic CMOS logic. Design an adiabatic 2 input AND/NAND.

SECTION C

3. Attempt any one parts of the following: **10 x 1 = 10**

a. Enlist the classification of CMOS digital logic families. Why CMOS VLSI design is better techniques than its counter parts?

b. What are the various processes of CMOS fabrication? Illustrate the main steps in a typical n-well process.

4. Attempt any one parts of the following: **10 x 1 = 10**

a) Prove that pull-up to pull-down ratio for an NMOS inverter driven by another NMOS inverter is 4/1. Implement the Boolean function f(A,B,C)=$\bar{A}$BC+A$\bar{B}$C+AB$\bar{C}$ using CMOS logic.

b) Explain the concept of MOSFET as switches with the help of diagram. Calculate the delay involved in cascaded pass transistors.

5. Attempt any one parts of the following: **10 x 1 = 10**

a) Derive and explain the working of CMOS inverter with its VTC characteristics. Also calculate the V_{OL}, V_{OH}, V_{IL}, V_{IH} and V_{TH} for the CMOS inverter.

b) Explain CMOS edge triggered flip flop with the help of input and output waveforms.

6. Attempt any one parts of the following: **10 x 1 = 10**

a) Discuss the operation of single stage shift register circuits Design a SR flip-flop using CMOS circuits.

b) What are the various sources of power dissipation in CMOS circuits? Discuss in detail the variable threshold CMOS circuits.

7. Attempt any one parts of the following: **10 x 1 = 10**

a) Design the circuit describe by Boolean function Y = A.(B+C)(D+E) using CMOS logic .calculate the equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that [W/L]=5 for pMOS transistor and [W/L]=2 for nMOS transistors.

b) Explain the following:
i) Ad-Hoc testable design techniques ii) Built- in self test (BIST) techniques