



(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 131703

Roll No.

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B. Tech.

(SEM. VII) (ODD SEM.) THEORY
EXAMINATION, 2014-15

VLSI DESIGN

Time : 3 Hours]

[Total Marks : 100

- Note :** (1) Attempt all questions.
(2) All questions carry equal marks.

1 Attempt any four parts of the following : 5×4

- (a) Define VLSI design methodology (Y Chart) and MOS Scaling.
- (b) Explain the CAD Tools for VLSI Design.
- (c) Discuss the classification of CMOS digital logic families.
- (d) Draw a 4×1 Multiplexer using Transmission Gate (TG).
- (e) For an n channel MOS transistor with

$$\mu_n = 60 \text{ cm}^2 \mu\text{A}/\text{V}^{-\text{s}}, \quad C_{ox} = 7 \cdot 10^{-8} \text{ F}/\text{cm}^2,$$

$$W = 20 \mu\text{m}, \quad L = 2 \mu\text{m} \quad \text{and} \quad V_{TO} = 1.0\text{V}.$$

Examine the relationship between the drain current and the terminal voltages.

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[Contd...

- (f) Explain the CMOS inverter switching characteristic and explain the definitions of delays and transition times.

2 Attempt any two parts of the following : 10×2

- (a) Enlist the Layout design process and design rules of CMOS circuit. Draw a stick diagram of CMOS NOR gate.
- (b) Consider a CMOS inverter circuits with the following parameters $V_{DD} = 3.3V$, $V_{Ton} = 0.6V$, $V_{Top} = -0.7V$, $k_n = 200 \mu A/V^2$, $k_p = 80 \mu A/V^2$, $k_R = 2.5$ Calculate the noise margin of the circuits.
- (c) Consider a CMOS inverter, with the following device parameters, $V_{DD} = 5V$, $V_{Ton} = 0.6V$, $V_{Top} = -0.7V$, $\mu_n C_{ox} = 60 \mu A/V^2$, $\mu_p C_{ox} = 20 \mu A/V^2$, $\lambda = 0$. Determine the $\left(\frac{W}{L}\right)$ ratios of the nMOS and the pMOS transistors such that the switching threshold is $V_{th} = 2.5V$.

3 Attempt any four parts of the following : 5×4

- (a) Discuss the Elmore Delay.
- (b) Discuss the classification of Dynamic CMOS logic families.
- (c) Discuss the operation of pass transistor in dynamic logic circuit.

- (d) In a logic Design logic function is
 $Z = \overline{(A+B+C+D)(E+F+G)(H+I)}$ implemented
 with domino CMOS circuits diagram with
 implements Z.
- (e) Discuss the overview of Power Consumption
 in CMOS logic circuits.
- (f) Design 2 input EXOR Logic Gate using
 CMOS Transmission Gate.

4 Attempt any two parts of the following : **10×2**

- (a) In a CMOS inverter power supply $V_{DD} = 5V$,
 determine the fall time, which is define as the
 time elapsed between the time point at which
 $V_{out} = V_{90\%} = 4.5V$ and the time point at
 which $V_{out} = V_{10\%} = 0.5$. The output load
 capacitance is 1pF. The nMOS transistor
 parameters are as follows : $V_{Tn} = 1.0V$,

$$\mu_n C_{ox} = 20\mu A/V^2, \left(\frac{W}{L}\right)_n = 10.$$

- (b) Design the circuit described by the Boolean
 function $Y = \overline{A \cdot (B + C)(D + E)}$ using CMOS
 logic. Calculate the equivalent CMOS inverter
 circuit for simultaneous switching of all inputs
 assuming that $\left(\frac{W}{L}\right) = 10$ for pMOS transistor
 and $\left(\frac{W}{L}\right) = 5$ for all nMOS transistor.

- (c) Discuss the operation of single stage shift register circuits. Design a SR flip-flop using CMOS circuits.

5 Attempt any four parts of the following : 5×4

- (a) Define the terms Controllability and Observability.
- (b) Explain the implementation of Built-In Self Test (BIST) design techniques for VLSI circuit testing.
- (c) Design a D flip-flop using CMOS Transmission Gate circuits.
- (d) Discuss the operation of CMOS SRAM cell circuit.
- (e) Write short notes on Adiabatic CMOS logic. Design an adiabatic 2 input AND/NAND.
- (f) Discuss the low power MTCMOS VLSI designs techniques.
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