(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 2728 Roll No. | | | | | | | | | | |

B.Tech.

(SEM. VII) ODD SEMESTER THEORY EXAMINATION 2013-14

VLSI DESIGN

Time : 3 Hours *Total Marks : 100*

Note :–Attempt **all** questions.

1. Attempt any **four** parts of the following : **(4×5=20)**
   (a) Discuss the Hierarchy of various semiconductor technology with Moore's and VLSI design flow.
   (b) Write an expression for power dissipation in CMOS inverter.
   (c) Write short notes on Mosfet Scaling and Channel Length Modulation.
   (d) Explain limitations of scaling in VLSI fabrication technology.
   (e) Explain the two kinds of design rules –micro rules and lambda rules.
   (f) Draw a stick diagram for 2 input NAND Logic Gate using CMOS Logic.
2. Attempt any **four** parts of the following : **(4×5=20)**
   (a) Prove that pull-up to pull-down ratio for an NMOS inverter driven by another NMOS inverter is 4/1.
   (b) Implement the Boolean function f(A,B,C)= $\overline{A}.BC + A\overline{B}C + AB\overline{C}$ using CMOS logic.

(c) Explain the concept of MOSFET as switches with help of diagram.

(d) Calculate the delay involved in cascaded pass transistors.

(e) Write a short note on Adibatic Low Power digital logic technique.

(f) Explain depletion Load Inverter with suitable sketch.

3. Attempt any **two** parts of the following : **(10×2=20)**

(a) Derive the expression for V_{IH}, V_{IL}, N_{ML} and N_{MH} for CMOS inverter.

(b) Explain two input XOR gate using CMOS logic circuits, TG gate and Pass Transistor logic.

(c) Explain CMOS edge triggered flip flop with help of input and output waveforms.

4. Attempt any **two** parts of the following : **(10×2=20)**

(a) Explain leakage currents in DRAM cells and refresh operation with help of schematic view, cross-section view and timing diagram.

(b) What is SRAM ? Explain CMOS SRAM cell design strategy.

(c) What is Flash Memory ? Explain NAND flash memory cell.

5. Attempt any **two** parts of the following : **(10×2=20)**

(a) Explain the following :

(i) Controllability and Observability

(ii) Scan Based Technique.

(b) Explain the following :

(i) Ad Hoc Testable design techniques

(ii) Fault types and models

(c) Explain the classification of Dynamic CMOS logic circuit and design a 2 input EXOR logic Gate using Domino logic.