

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 2728

Roll No.

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B.Tech.

(SEM. VII) THEORY EXAMINATION 2011-12

VLSI DESIGN

Time : 3 Hours

Total Marks : 100

Note :- (1) Attempt **All** questions.

(2) **All** questions carry equal marks.

- Attempt any **two** parts of the following : **(10×2=20)**
 - Discuss the hierarchy of various semiconductor technology with Moore's law and VLSI design flow (Y chart).
 - Explain the structure and operation of MOS transistor. What is meant by Z_{pu} and Z_{pd} in the inverter circuit ? Derive the required ratio between Z_{pu} and Z_{pd} , if a MOS inverter is to be driven from another n-MOS inverter.
 - Explain n-MOS Fabrication with suitable sketch.
- Attempt any **two** parts of the following : **(10×2=20)**
 - Write short notes on the following :
 - MOSFET Scaling
 - Channel Length Modulation.
 - Derive the expression for V_{IH} , V_{IL} , NM_L and NM_H for CMOS inverter.

- (c) Design a 2 input XOR logic using CMOS Transmission Gate and compare with Pass transistor and CMOS logic circuit.
3. Attempt any **four** parts of the following : **(5×4=20)**
- (a) Explain the behavior of Pass transistor in dynamic CMOS logic implementation.
 - (b) Draw a CMOS shift register circuit.
 - (c) Explain the effect of constant voltage scaling on Delay and Power Delay Product (PDP).
 - (d) What are the various sources of power dissipation in CMOS circuits ?
 - (e) Explain how DOMINO CMOS logic overcomes the charge sharing problem.
 - (f) Explain the term Voltage Bootstrapping in CMOS logic with suitable example.
4. Attempt any **two** parts of the following : **(10×2=20)**
- (a) Enlist the advantage of dynamic logic circuit over static logic circuit. Explain DOMINO and NORA CMOS logic circuit with suitable example.
 - (b) Write a short note on DRAM cells. Explain leakage currents and refresh operation in DRAM cells.
 - (c) Discuss with a neat diagram the operation of CMOS SRAM cell.

5. Attempt any **two** parts of the following : **(10×2=20)**
- (a) Write a short note on adiabatic logic circuit. Differentiate between single struct-at fault and multiple struct-at fault.
 - (b) Define the terms Controllability and Observability. Discuss in brief Ad-hoc Testable design techniques.
 - (c) Briefly explain the issues involved in Built-in Self Test (BIST) techniques.