

(Following Paper ID and Roll No. to be filled in your Answered in CMOS

PAPER ID : 3042

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B.Tech.

RET

SIXTH SEMESTER EXAMINATION, 2004-2005

VLSI - TECHNOLOGY

Time : 2 Hours

Total Marks : 50

Note : Attempt ALL the questions.

1. Attempt *any four* of the following : 5x4=20
- Describe the atom density for the principal planes of GaAs in terms of cube edge? How is the bond density calculated for these planes?
 - What is the equilibrium concentration of Schottky defects in Silicon at 300 and 1500 k? Repeat for frenkel defects and compare the numbers.
 - How are single crystals grown? Describe one of the approaches that allow the crystal to be grown with a free surface?
 - A small silicon bar is doped with boron and antimony. One end of bar is inserted into a furnace and melted. The bar is now withdrawn. Sketch the doping profile that results from the regrowth process and calculate the base width of the resulting transistor? Assume equilibrium values for k, and that the original antimony/boron atom ratio was 33.

- (e) Discuss the operations performed during wafer preparation ? What are the precautions that must be taken ?
- (f) Describe Cz furnace. What are its advantages ?

Attempt *any four* of the following : 5x4=20

- (a) Describe "Dopant profiles" in brief.
- (b) What is the photo lithography technique ? Discuss in brief.
- (c) Describe Doping and Autodoping in the growth process ?
- (d) By giving a clear schematic, describe the Molecular Beam Epitaxy (MBE) growth system.
- (e) How are epitaxial slices evaluated for doping and thickness ? Describe in brief.
- (f) Discuss the salient properties of silicon dioxide, in brief.

Attempt *any two* of the following : 10x2=20

- (a) What do you understand by "Process Simulation" ? Discuss in brief.
- (b) Discuss and describe the Boltzmann Transport Equation Approach and Monte Carlo Methods of Ion Implementation in brief.
- (c) Write short note on Interfaces, Channeling and lateral effects in Boltzmann Transport Equation Approach (BTE) and Monte Carlo (MC) models.

4. Attempt *any two* of the following : 10x2=20

- (a) What is latchup ? How is latchup avoided in CMOS technology ? Support your answer with requisite mathematical expressions.
- (b) What are the effects of nesting tolerances on MOSFET layout ? Discuss and describe with the help of suitable diagrams.
- (c) Discuss and describe the basic design rules for miniaturizing VLSI circuits, in brief.

5. Write short notes on *any two* of the following : 10x2=20

- (a) Fabrication technique for poly silicon gate P channel devices.
- (b) IIL circuit fabrication
- (c) MOSIC fabrication techniques.