E-T- VI

Roll No. ☐☐☐☐☐☐☐☐☐☐

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EC-605

B. TECH.

SIXTH SEMESTER EXAMINATION, 2002-2003

VLSI-TECHNOLOGY

Time : 2 Hours *Total Marks : 50*

Note : Attempt **ALL** the questions.

1. Attempt any FOUR of the following :— (3×4=12)

   (*a*) Explain, briefly, the zone refining process used for silicon crystal growth.

   (*b*) Explain, why extremely rapid initial growth is observed during dry oxidation and is totally unnoticed during wet oxidation.

   (*c*) Explain the applications of SiO_2 layer in Ic fabrication.

   (*d*) Explain the process of oxidation and describe the oxidation furnace used for it.

   (*e*) Differentiate between Bipolar and MOS Ic technology.

   (*f*) Explain the wafer processing technique used in Ic technology.

2. Attempt any FOUR of the following :— (3×4=12)

   (*a*) What types of diffusion are used for the following regions of BJT ? Why ?

   (*i*) Emitter

   (*ii*) Base

   (*b*) Explain, why boron and phosphorus are preferred for *p* and *n* diffusions of silicon respectively compared to other materials.

(*c*) Mention different advantages of ion implantation over diffusion.

(*d*) Explain the EPITAXIAL LAYER GROWTH and its significance in Ic technology.

(*e*) Explain the lift-off technique. Where is it used ?

(*f*) Explain, briefly, the various steps of optical lithography.

3. Attempt any TWO of the following :— **(6.5×2=13)**

(*a*) Explain, why sputtering is needed for the deposition of refractory materials like tantalum.

With a neat diagram, explain the D. C. sputtering technique.

(*b*) Explain, with neat diagram, the fabrication of BJT by double diffused epitaxial process.

(*c*) Give reasons and explain why *npn* transistors are preferred over *pnp* counterpart.

4. Attempt any TWO from the following :— **(6.5×2=13)**

(*a*) Define threshold voltages for an enhancement and a depletion mode MOSFET. Discuss the working of an enhancement *n*-type MOSFET.

(*b*) Derive an expression for the ID-VDS characteristics of an enhancement *n*-channel MOSFET in the resistive region using gradual channel approximation. Deduce the expression for the saturation region.

(*c*) Explain, with a neat diagram, the fabrication of a MOSFET using self-aligned poly-gate technology.

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