Printed Pages – 3 TEC – 603

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3093 Roll No. | | | | | | | | | | |

B.Tech.

(SEM VI) EVEN SEMESTER THEORY EXAMINATION, 2009-2010

VLSI TECHNOLOGY AND DESIGN

Time : 3 Hours *Total Marks : 100*

Note : *Attempt **all** questions.*

1. Attempt **any four** parts of the following : **(4x5=20)**

   (a) Define the term IC. List its types. How does analog ICs' differ from digital ICs' ?

   (b) In Bipolar IC the transistor are suitable connected to act as diode. How many ways are there to connect transistor to form a monolithic diode ?

   (c) Show that thickness of oxide during growth is directly proportional to time for small oxidation time.

   (d) Explain why extremely rapid growth is observed during wet oxidation compared to dry oxidation ?

(e) A thin film capacitor has a capacitance of 0.4 pF/mil^2. The relative dielectric constant of SiO_2 is 3.5. What is the thickness of SiO_2 layer in angstroms ?

(f) Explain the various techniques to form oxide layer and describe the applications of oxide layer.

2. Attempt **any two** parts of the following : **(2x10=20)**

(a) Why is diffusion needed to form a bipolar transistor ? Explain with each diffusion step. What is the equilibrium concentration of Schottky defects in Si at 300 K ?

(b) Write short notes on :

(i) Annealing

(ii) Epitaxy

(c) What are photo resist materials ? Describe types of photo resists. What are the requirements of oxide used for a mask in photolithography ?

3. Attempt **any four** parts of the following : **(4x5=20)**

(a) What is the advantage of polysilicon gate over metal gate ? How is it fabricated ?

(b) Describe the operation of a basic MOS inverter. Derive the expression for a pull up to pull down ratio for an N MOS inverter.

(c) Define the threshold voltage and derive the expression for V_{th} in a MOS transistor.

(d) Draw a CMOS inverter and explain its transfer characteristics.

(e) Realize the expression $Y = \overline{A\,(D + E) + BC}$ using nMOS transistor.

(f) Draw the circuit diagram of one stage of a dynamic CMOS register.

4. Attempt **any two** parts of the following : **(2x10=20)**

(a) Draw a stick diagram for a two input multiplexed latch, using the two transmission gate side by side.

(b) Discuss the architecture of FPGA. How FPGA programmed ?

(c) (i) Sketch the circuit diagram of a ratio less MOS inverter and explain its operation.

(ii) Discuss the operation of a 4 cell MOS RAM.

5. Attempt **any two** parts of the following : **(2x10=20)**

(a) Describe the lambda design rules and layout methodology for CMOS circuit design.

(b) Discuss programmable logic array (PLA) with example of NMOS PLA.

(c) Write a short note on VLSI testing.

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