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Printed Pages : 3 **TEC – 603**

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3093 Roll No. | | | | | | | | | | |

B. Tech.

(SEM. VI) EXAMINATION, 2006-07

VLSI TECHNOLOGY & DESIGN

Time : 3 Hours] *[Total Marks : 100*

Note : *Attempt **all** questions.*

1 Attempt any **four** parts of the following : **5×4=20**

(a) Discuss different steps in preparing wafers from raw silicon.

(b) Why cleaning of silicon wafers is necessary before any processing steps? What are clean room standards?

(c) Why (100) orientation is preferred over (111) orientation for starting material in NMOS/ CMOS ICS fabrication.

(d) List non-ideal I-V effects in MOS and explain them briefly.

(e) Discuss Gate capacitance model and diffusion capacitance model of MOS.

(f) Compare voltage levels and noise margin for bipolar and CMOS logic family.

2 Attempt any **four** parts of the following : **5×4=20**

(a) What are the requirements of a photoresist? Which photoresist is preferred for better resolution and why?

(b) Compare horizontal tube furnace with vertical tube furnace for oxidation.

(c) Why Ion-implantation is preferred over diffusion for impurity doping? Explain briefly ion-implantation technique.

(d) What is epitaxy? Discuss any one type of epitaxy method briefly.

(e) List and compare different types of lithography techniques.

(f) What are the limitations of pure aluminium metallisation for sub-micron level devices ?

3 Attempt any **two** parts of the following : **10×2=20**

(a) Explain CMOS Inverter Voltage transfer characteristic with a neat diagram. What is the criteria for voltage threshold for high level and low level in inverter characteristic?

(b) Explain CMOS inverter layout plan alongwith its cross-sectional diagram. What is a stic diagram? What do you mean by Lemda based design rule ?

(c) Explain different levels in device models. What is device characterisation and circuit characterisation with reference to circuit simulation ?

4 Attempt any **two** parts of the following : **10×2=20**

(a) Explain read/write operation of SRAM memory cell. How 1 bit cell is used in bigger memory systems?

(b) Explain basic organisation of nMOS NAND ROM and its layout. Compare different types of ROM structures.

(c) Explain technology related CAD issues. What do you mean by Design Rule Checking (DRC) and circuit extraction?

5 Attempt any **four** of the following : **5×4=20**

(a) Discuss briefly testing and verification of VLSI circuits.

(b) What do you mean by silicon debug principles? Explain briefly test benches and hardnesses.

(c) Compare FPGA with CPLD. How a processor chip can be designed using FPGA ?

(d) Explain system-on a-chip concept using platform based design.

(e) Explain briefly structured design techniques.

(f) What is an Application Specific Integrated Circuit? Give examples of ASIC.
