**Printed Pages : 3**

**EEC027**

(Following Paper ID and Roll No. to be filled in your Answer Book)

**PAPER ID : 121652**

**Roll No.**

# B. Tech.

## (SEM. VI) THEORY EXAMINATION, 2014-15

## VLSI DESIGN

Time : **2** Hours] [Total Marks : **50**

**Note:** All questions are compulsory.

**1** Attempt **any four** parts: **3.5×4=14**

(i) Explain the steps involved in fabrication of CMOS twin-tub process.

(ii) Explain the trends of scaling in VLSI fabrication technology.

(iii) How BICMOS technology is better than CMOS technology ?

(iv) What is body bias effect and how it affects MOSFET operation ?

(v) Derive the expression for Drain current in MOSFET.

(vi) Define figure of Merit of MOSFET transistor and explain how $g_m$ is related to drain current and aspect ratio of MOSFET.

**2** Attempt **any two** parts: **6×2=12**

(i) Draw the layout of two input NAND gate. Explain symbol, different colors and lines used for drawing stick diagram of NAND gate.

(ii) Derive the expression for fall time and rise time for CMOS inverter.

(iii) A CMOS inverter circuit with parameters, $V_{DD} = 2V$, $V_{T0}$, n = 0.4V, $V_{T0}$, p = −0.4V, $K_n = 250\mu A/V^2$, $K_p = 90\ \mu A/V^2$. Calculate the Noise margin of the circuit assuming CMOS inverter has $K_R = 1.5$ and $V_{T0}$, $n \neq |V_{T0,}p|$.

**3** Attempt **any two** parts: **6×2=12**

(i) Explain the behavior of bistable elements. Explain the working of CMOS NOR based clocked JK latch.

(ii) What are the approaches for Structural to Layout synthesis ?

(iii) Explain BIST process and its implementation with block diagram.

**4** Attempt any two parts: **6×2=12**

(i) What is Scan path testing and how it is different from Boundary scan testing?

(ii) Explain the concept of regularity, modularity, semi-custom and full custom styles of VLSI system design.

(iii) Describe the concept of PLA and FPGA with reference to VLSI Design.