(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 2484 Roll No. | | | | | | | | | | |

B. Tech.

(SEM. VI) THEORY EXAMINATION 2011-12

VLSI DESIGN

Time : 2 Hours *Total Marks : 50*

Note : Attempt ***all*** questions. All questions carry marks as indicated.

1. Attempt any ***four*** parts of the following : **(4×3=12)**

   (a) Differentiate between a discrete component circuit and an integrated circuit. Classify the ICs on the basis of scale of integration.

   (b) Give the speed/power performance comparison of available semiconductor technologies such as nMOS, CMOS, BiCMOS, ECL, TTL, GaAs technologies.

   (c) Sketch the cross-section and explain the operation of an n-channel depletion type MOS transistor. Draw the drain characteristics and its transfer curve.

   (d) How many diffusions are needed to form an nMOS transistor ? Explain the purpose of each diffusion step.

   (e) What are the different methods for CMOS fabrication ? Explain any one of them in detail.

   (f) Define transconductance and output conductance of MOS transistor. Also find expression for transconductance.

2. Attempt any ***two*** parts of the following : **(2×6=12)**

   (a) Draw the different types of MOS inverter circuits and their transfer characteristics. Compare their relative advantages and disadvantages.

(b) Describe the stick layout design style for CMOS circuit design.

(c) Draw CMOS inverter circuit and explain its transfer characteristics. If the change over between logic levels is symmetrical, show that the width to length ratio of the p-device is approximately three times that of the n-device.

Attempt any ***two*** parts of the following : **(2×6=12)**

(a) What is VLSI design rule ? Why is it required ? Describe the Lambda based design rules for CMOS circuit design. Explain with suitable diagram.

(b) Construct a colour coded stick diagram to represent the design of a CMOS circuit that implements the following function :

$$F = \overline{A} \cdot (\overline{B} + \overline{C}).$$

(c) Discuss a combined voltage and dimension scaling model. Compare the scaling factors for the following device parameters :

Gate area, Gate capacitance, channel resistance, current density and power dissipation for the different scaling models.

4. Attempt any ***two*** parts of the following : **(2×7=14)**

(a) Describe the standard cell based design. Enlist the various standard cell library. What are the parameters of good VLSI design ?

(b) Design an n-MOS switch based logic implementation of a four-way multiplexer layout.

(c) Draw and discuss the general format of Built-in-Self-Test (BIST) structure.