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Sub Code: NEC-024R

Paper Id:

131634

Roll No:

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B.TECH
(SEM VI) THEORY EXAMINATION 2017-18
ADVANCED DIGITAL SYSTEM DESIGN USING VERILOG

*Time: 3 Hours**Total Marks: 100*

- Note:** 1. Attempt all Sections.
 2. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x10 = 20**
- a. What do you understand by identifiers and memory operators?
 - b. Draw a simulation flow chart.
 - c. What do you understand by assignments with delays?
 - d. What is sequential circuit testing?
 - e. What are the differences between behavioral modeling and switch level modeling?
 - f. Define initial construct.
 - g. Distinguish between a task and a function.
 - h. What are test bench techniques?
 - i. What is fault detection?
 - j. Define bidirectional gates.

SECTION B

2. Attempt any *three* of the following: **10 x 3 = 30**
- (a) With the help of suitable examples explain concurrent and procedural statements with syntaxes. Also with the help of block diagram explain the components of a verilog module.
 - (b) What is a tri- state gate and explain each type of tri state gate with truth tables. Also design module and a test bench for a half adder?
 - (c) Discuss the differences between blocking and non blocking assignments with suitable examples. Design a half adder using CMOS switches. What are basic switch primitives?
 - (d) What do you understand by user defined primitives (UDP) and explain their types with suitable examples.
 - (e) With the help of suitable examples explain the concept of formal verification of a system. Also explain the use of assert cycle sequence and assert next with suitable examples.

SECTION C

3. Attempt any *one* part of the following: **10 x 1 = 10**
- (a) What is the need for synthesis? Briefly discuss the two common approaches for hardware realization using synthesis tool. Also write the structure of typical simulation module and explain.
 - (b) Explain different data types in verilog HDL. Also discuss the different driving strengths in verilog with strength level, key board and element modeled.

4. **Attempt any *one* part of the following:** **10 x 1 = 10**
- (a) Explain 'wand' and 'wor' types of nets with examples. Also explain NAND gate primitive with verilog module.
- (b) Draw a 3 to 8 decoder using 2 to 4 decoder and write the verilog module for the same.
5. **Attempt any *one* part of the following:** **10 x 1 = 10**
- (a) Design a module for 4 bit four functions ALU and also a test bench for the same by using behavioral modeling.
- (b) Design a 2:4 demultiplexer module and test bench using the if-else-if construct in a verilog.
6. **Attempt any *one* part of the following:** **10 x 1 = 10**
- (a) Explain why 'specparam' construct is used in specify block? Distinguish between 'specparam' and 'parameter'. Also explain recursive function with example.
- (b) Briefly explain feedback model and a capacitive model with suitable examples. Also write verilog module for D latch using UDP.
7. **Attempt any *one* part of the following:** **10 x 1 = 10**
- (a) Draw the basic functional unit of a dynamic shift register using switch level modeling. Also write verilog module and test bench.
- (b) With the help of suitable examples briefly explain BDD, ordered BDD and LPDD. Also write the differences between them.