02357

Printed Pages—4 **EC—501**

(Following Paper ID and Roll No. to be filled in your Answer Book)										
PAPER ID : 3004	**Roll No.**									

B.Tech.

FIFTH SEMESTER EXAMINATION, 2005-2006

DIGITAL INTEGRATED CIRCUITS

Time : 3 Hours *Total Marks : 100*

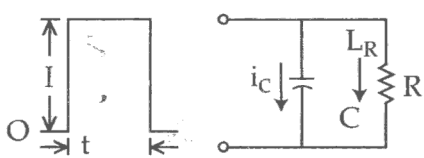
Note : *(i) Attempt **ALL** questions.*

(ii) All questions carry equal marks.

(iii) Be precise in your answer.

1. Attempt ***any four*** parts of the following : **(5x4=20)**

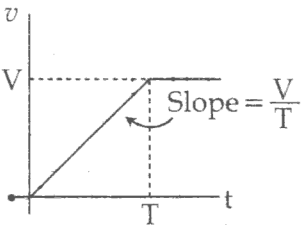
(a) A current pulse of amplitude I is applied to a parallel RC circuit as shown in figure below, plot to scale (approximately) wave forms of currents i_c, for the cases (i) $t < RC$ (ii) $t = RC$ and (iii) $t > RC$



(b) A symmetrical square wave of peak-to-peak amplitude V and frequency f is applied to a high pass RC circuit. Show that percentage tilt is given by

$$P = \frac{1-e^{-\frac{1}{2}/RC}}{1+e^{-\frac{1}{2}/RC}} \times 200\%.$$

(c) A ramp as shown in figure is applied to a RC differentiates. Draw the output waveform for the cases :

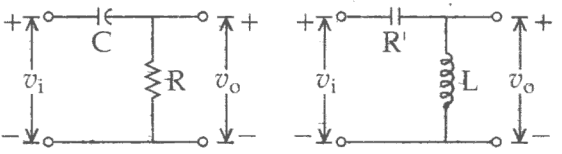


(i) $T = RC$

(ii) $T = 0.2\ RC$

(iii) $T = 5RC$

(d) Prove that for same input and with circuits at rest, the output from both differentiating circuits will be same if $RC = L/R'$.



(e) Why integrators are preferred over differentiates in analog computer applications.

(f) Why compensation is required in attenuator at all ? Draw step responses of over compensated and under compensated attenuators and explain.

2. Attempt *any four* parts of following : 5x4=20

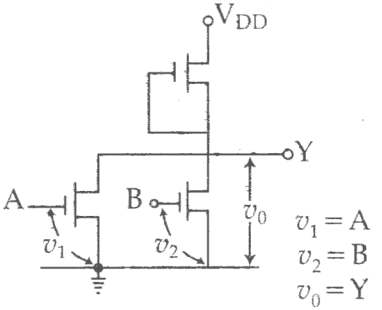
(a) Compare the relative merits of N MOS, C MOS, TTL and ECL logic families.

(b) Draw the circuit diagram of a TTL NAND gate and explain its operation.

(c) Draw the circuit diagram of a CMOS NOR gate, explain its operation and enumerate five desirable properties of CMOS gates.

(d) Draw the circuit diagram of a ECL OR/NOR gate, explain its operation and discuss the significance of reference voltage.

(e) For the circuit shown below, find output boolian expression for Y and hence deduce the truth table.



(f) List and discuss four advantages and four disadvantages of a the ECL gate.

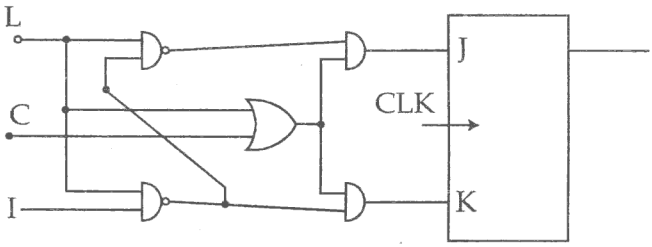
3. Attempt *any two* parts of following : **10x2=20**

(a) What do you mean by universal shift register ? Draw the circuit diagram of a universal shift resistor and explain its working with timing diagram.

(b) What is the difference between serial and parallel transfer ? Explain how to convert serial date to parallel and parallel data to serial. What type of register is needed.

The content of a 4 bit register is initially 1101. The register is shifted to six times to the right with serial input being 101101. Tabulate the content of each register after each shift.

(c) For the figure shown below, derive the flip-flop input equations for J and K in terms of L, C and I. Explain the working of circuit.



4. Attempt *any two* parts of following :

(a) Differentiate between DRAM and SRAM. Draw the logic diagram of a memory cell (RAM) and explain its working with read and write timing diagram.

(b) Draw the wiring diagram of 256K byte ROM bank using $32K \times 8$ ROM chip and mention (i) Number of address lines (ii) Specify decoder.

(c) Draw the circuit diagram of Schmitt trigger circuit using 555 explain its operation with suitable waveforms. Enumerate the application of this circuit.

5. Write short notes on *any three* of following : 20

(a) Multiplexer and Demultiplexer

(b) PLA and PAL

(c) SPLD and CPLD

(d) As table and mono stable multivibrator

(e) BiCMOS digital circuit.

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