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No. of Printed Pages—5 **EC–501**

B. TECH.

FIFTH SEMESTER EXAMINATION, 2003-2004

DIGITAL INTEGRATED CIRCUIT

Time : 3 Hours *Total Marks : 100*

Note : Attempt **ALL** questions.

1. Attempt any FOUR parts of the following :—

(a) Describe a low pass passive RC filter. Derive the expression for its transfer function. Draw its characteristics.

(b) Describe the circuit of a RC high-pass filter which can be used as a differentiator. Derive the transfer function. Draw the waveforms of the output voltage for different values of time constant when the input is a square waveform.

(c) Draw the RC circuit for Compensated Attenuator. A simple RC low-pass filter is to be designed that the output voltage be attenuated by 3 db at 50 Hz. Calculate the time constant and suitable value of R and C.

(d) Explain the Diode Reverse Recovery Time.

(e) Sketch the waveform for collector current, i_c, of fig. (1·1) if maximum (saturation) current $I_{CS} \approx \frac{V_{CC}}{R_L}$. Also clearly indicate the turn ON (t_{ON}) time and turn OFF (t_{OFF}) time on the collector current response.

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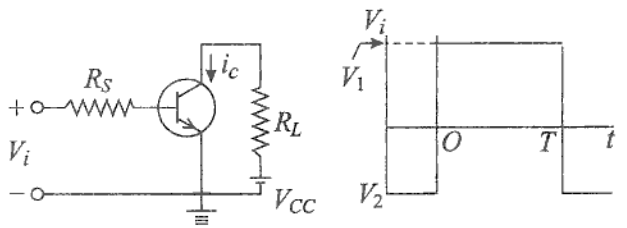


Figure–(1·1)

(f) Consider the circuit, shown in fig. (1·2) which uses TTL gates. The current I is 1·6 mA when terminal B is left unconnected. Find the value of I when B is connected to A. Comment on the effect of this connection on the fan-out of gate G_1.

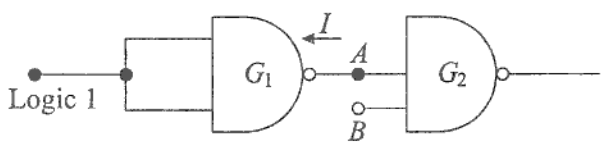


Fig.(1·2)

2. Attempt any FOUR parts of the following :—

(a) How does Transitor-Transitor Logic (TTL) gate differs from MOS gate ?

(b) Draw the circuit of a ECL gate and explain its operation.

(c) Draw the circuit for CMOS Inverter. Three CMOS devices are cascade. If each has a propagation delay time of 100 ns, what is the total propagation delay time ?

(d) Explain the working of Integrated-Injection Logic (IIL).

(e) What are the different schemes for CMOS-to-TTL interface ? Explain one of them.

(f) Define the following terms :—

(i) Noise Immunity

(ii) Power Dissipation per gate

(iii) Propagation Delay Time

3. Attempt any TWO parts of the following :—

(a) Draw the block diagram of Serial In-Parallel Out Shift Register and explain its operation. Also write down the applications of shift register.

(b) Explain the following :—

(i) Bidirectional Shift Register

(ii) Modulus of the Counter

Design a 3-bit synchronous counter using J-K flip-flop.

(c) Draw the block diagrams of digital Multiplexer and Demultiplexer and explain. An 8×1 Multiplexer has inputs A, B and C connected to the selection input S_2, S_1 and S_0 respectively. The data inputs I_0 through I_7 are as follows :

$I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$ & $I_6 = D'$.

Determine the Boolean function that the Multiplexer implements.

4. Attempt any TWO parts of the following :—

(a) Explain the operation of writing a word into the selected memory location and reading the content of a selected memory location. Draw the diagram for M×N sequential memory and explain.

(b) Explain the following :—

(i) Dynamic MOS RAM Cell

(ii) Memory Addressing

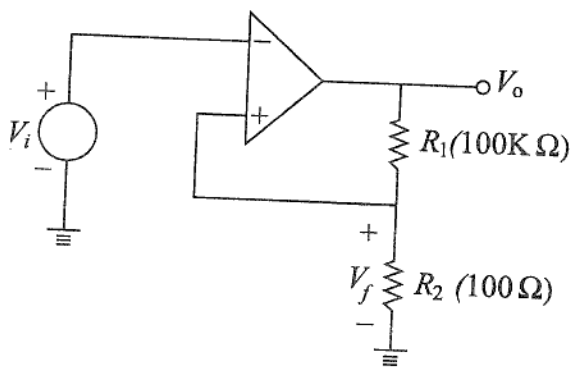
(iii) Monostable Multivibrator.

(c) Draw the functional block diagram of 555 time and explain its operation.

In the Schmitt Trigger Circuit of fig. (4·1),

(i) if $V_{Sat} = 13V$, find the Upper Triggering Voltage (V_{UT}) and Lower Triggering Voltage (V_{LT}).

(ii) if $V_i = 5 \sin \omega t$, find the waveform of the output Voltage.



Figure–(4·1)

5. Attempt any TWO of the following :—

(a) Draw the block diagram of a PLA device and explain its operation. How will you expand PLA capacity.

(b) Draw the basic configuration of three PLDs and explain in brief. Also differentiate between GaAs based circuit and Bi CMOS circuit.

(c) Draw the logic configuration of four input and four output PAL and explain.

Also explain the field programmable gate array (FPGA).

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