Roll No. | | | | | | | | | | |

No. of Printed Pages—4 **EC—501**

B. TECH

FIFTH SEMESTER EXAMINATION, 2002-2003

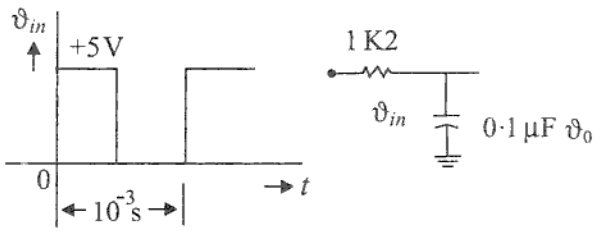
DIGITAL INTEGRATED CIRCUITS

Time : 3 Hours *Total Marks : 100*

Note : Attempt **ALL** questions.

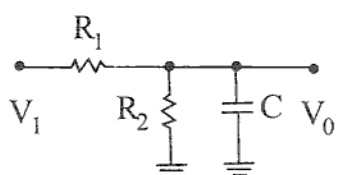
1. (*a*) Attempt any TWO of the following :— **(5×2)**

(*i*) Draw the output waveform for the following circuit with input shown on the same time scale.



(*ii*) Explain with proper reasons, why compensated CRO probes are recommended to be used.

(*iii*) Calculate the output voltage for the following circuit :—



(*b*) Attempt any TWO of the following :— (5×2)

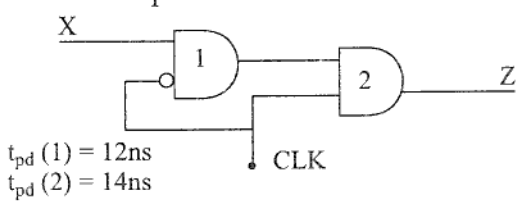
(*i*) Draw the interconnection of I^2L gate to form a 2×4 decoder.

(*ii*) Explain how a MOS can be used as a switch in a digital circuit.

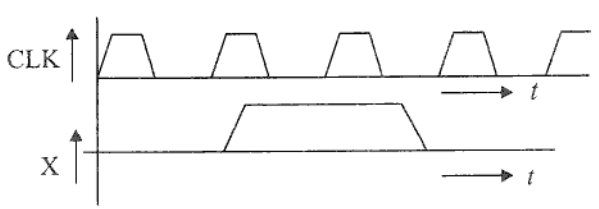
(*iii*) Justify the requirements of interfacing circuits between circuits of two different logic families and draw interfacing circuit required between TTL and CMOS gates.

2. Attempt any FOUR from the following :— (5×4)

(*a*) Draw the output waveform for the following circuit with input shown on same time scale :



t_{pd} (1) = 12ns
t_{pd} (2) = 14ns

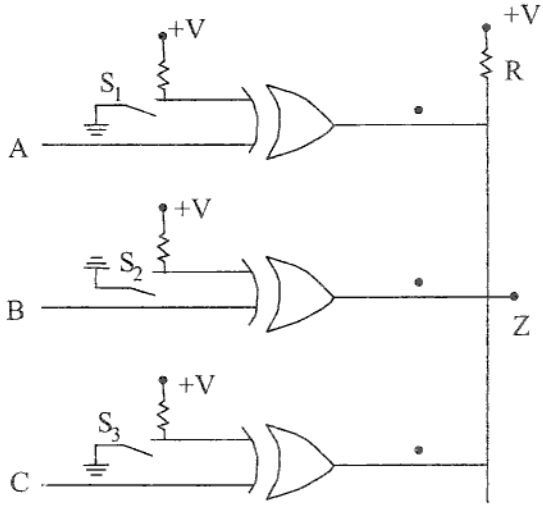


(*b*) Draw the internal structure of a TTL tri-stated gate and explain its operation.

(*c*) Explain with proper reasons, why ACTIVE pull up and pull down are preferred over PASSIVE in a TTL.

(*d*) Draw the output waveform of a BJT switch with a pulse input and explain valid reasons for the waveform deviation.

(*e*) Write TRUE expression for the following circuit :—



(*f*) Draw the internal structure of a CMOS inverter and derive the expression for P_D.

3. Attempt any TWO from the following :— **(10×2)**

(*a*) Design a Shift Register Counter to generate a sequence length of 8 having self-start feature.

(*b*) Realise the following boolean expression, using 4 : 1 MUX(s) only :—

$$Z = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,BC\overline{D} + A\overline{B}CD + A\overline{B}C\overline{D} + A\overline{B}\,\overline{C}\,\overline{D} + ABCD$$

(*c*) It is required that on POWER UP 1000 0000 should be loaded in an 8 bit Shift register. Data, thus loaded, should be shifted RIGHT through a '1' upon each rising edge of a clock applied. After 8 clock pulses, 1000 0000

should be reloaded in the counter and the action should be repeated (i.e., data should be shifted through '1' upon clock). Design a circuit to meet the requirement.

4. Attempt any TWO from the following :— (10×2)

(*a*) Design a 4×4 b RAM using D FFs and explain its working with proper timing diagram.

(*b*) For the window airconditioner installed in your digital lab., it is required that whenever switched ON, it will run on FAN for the first 3 minutes and the compressor will be ON thereafter. Suggest a scheme using 555 timer.

(*c*) (*i*) Explain Two-dimensional Selection Arrangement of ROM organisation.

(*ii*) Draw the circuit diagram of Schmitt trigger circuit and explain its working with the help of suitable waveforms.

5. Write short notes on any TWO of the following :— (10×2)

(*a*) GaAs-based circuits

(*b*) FPGA

(*c*) PLA