PAPER ID-411024

Subject Code: KEC051

Roll No: | | | | | | | | | | | | | |

# B TECH.
## (SEM V) THEORY EXAMINATION 2021-22
## COMPUTER ARCHITECTURE AND ORGANIZATION

***Time: 3 Hours*** ***Total Marks: 100***

**Note: 1.** Attempt all Sections. If require any missing data; then choose suitably.

### SECTION A

**1. Attempt *all* questions in brief.** **2 x 10 = 20**

| Qno. | Question | Marks | CO |
|---|---|---|---|
| a. | Write short note on PLDs. | 2 | 1 |
| b. | Define design methodology. | 2 | 1 |
| c. | Explain one, two, and three address instruction. | 2 | 2 |
| d. | Discuss Floating point number representation. | 2 | 2 |
| e. | Analyze overflow conditions for addition and subtraction. | 2 | 3 |
| f. | What is meant by ALU fast multiplication? | 2 | 3 |
| g. | What is interrupt? | 2 | 4 |
| h. | What do you mean by pipelining? | 2 | 4 |
| i. | Explain the concept of memory transfer. | 2 | 5 |
| j. | What is Cache? | 2 | 5 |

### SECTION B

**2. Attempt any *three* of the following:**

| Qno. | Question | Marks | CO |
|---|---|---|---|
| a. | Explain the general register organization with the help of suitable diagram. | 10 | 1 |
| b. | Describe fixed point representation and floating-point representation. | 10 | 2 |
| c. | Examine with a neat block diagram how floating-point addition is carried out in a computer system. | 10 | 3 |
| d. | Explain single cycle and pipelined performance with examples. | 10 | 4 |
| e. | A computer employs RAM chips of 256×8 and ROM chips of size 1024×8. Extend the memory system to 4096 bytes of RAM and 4096 bytes of RAM. List the memory address map and indicate what size decoders are needed? | 10 | 5 |

### SECTION C

**3. Attempt any *one* part of the following:**

| Qno. | Question | Marks | CO |
|---|---|---|---|
| a. | Discuss about advantages and disadvantages of PLD's. Design a 4-bit register with parallel I/O and 4-bit register with parallel load. | 10 | 1 |
| b. | A computer has 16-bit address and 16-bit data-lines.<br>i. What is maximum address space?<br>ii. What is size of each location in bytes?<br>iii. What is size of PC, AR, DR, IR? | 10 | 1 |

**4. Attempt any *one* part of the following:**

| Qno. | Question | Marks | CO |
|---|---|---|---|
| a. | Draw and explain typical micro programmed controller. What is program control unit? Design a state transition graph for the accumulator-based CPU with an example. | 10 | 2 |
| b. | Write a program to evaluate arithmetic expression<br>X= ( A – B ) * ( ( ( C -D ) / F) / G )<br>Using a general register computer with three, two, one & zero address instructions. | 10 | 2 |

**5. Attempt any *one* part of the following:**

| Qno. | Question | Marks | CO |
|---|---|---|---|
| a. | Explain how Booth's algorithm is suitable for signed number multiplication. Explain the floating-point multiplication with the help of flowchart. | 10 | 3 |
| b. | What are high speed adders? Design a Carry Look ahead adder. | 10 | 3 |

**6. Attempt any *one* part of the following:**

| Qno. | Question | Marks | CO |
|---|---|---|---|
| a. | Describe the following control units<br>i. Hardwired control unit<br>ii. Micro-programmed control unit | 10 | 4 |
| b. | Discuss the following<br>i. Interleaving<br>ii. Hit rate and Miss penalty<br>iii. Pre-fetching | 10 | 4 |

**7. Attempt any *one* part of the following:**

| Qno. | Question | Marks | CO |
|---|---|---|---|
| a. | Explain VHDL. What is device modeling? What are complier and simulator? Explain structural modeling with an example. | 10 | 5 |
| b. | What is Cache Memory? How is it implemented? A two way set associated 'cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is l28K x32.<br>i. Formulate all pertinent information required to construct the cache memory.<br>ii. What is the size of cache memory? | 10 | 5 |