(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 131402 **Roll No.** | | | | | | | | | | |

B.Tech.

(SEM. IV) THEORY EXAMINATION 2013-14

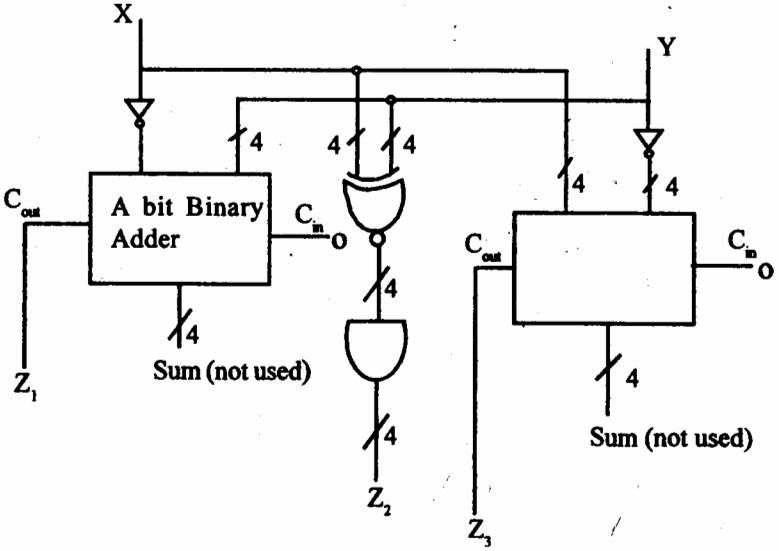
COMPUTER ARCHITECTURE AND ORGANIZATION

Time : 3 Hours *Total Marks : 100*

Note :– Attempt **all** questions. All questions carry equal marks.

1. Attempt any **two** parts of the following : **(2×10=20)**

(a) Name the circuit shown in figure 1, and relation between Input X.Y and output Z_1, Z_2, Z_3.



(b) Draw Truth table of full subtractor and implement using multiplexes.

(c) Implement the sequential circuit Sc using D flip-flop and NAND gates. Also draw the Truth table.

2. Attempt any **two** parts of the following : **(2×10=20)**

(a) Draw the functional block diagram of accumulator based CPU. Explain its operation and enumerate its instruction set.

(b) Differentiate between RISC and CISC type processor. How the performance of accumulator based CPU can be improved ?

(c) Draw the block diagram (organizational) of ARM 6 processor and explain its working.

3. Attempt any **two** parts of the following : **(2×10=20)**

(a) Draw the circuit diagram of two's complement multiplier and explain its working.

(b) Design a complete Two's complement adder subtractor.

(c) Construct a divider array for 3 bit unsigned numbers using call D, and explain its working.

4. Attempt any **two** parts of the following : **(2×10=20)**

(a) What do you mean by Hardwired and micro programmed control unit ? Show the organization of a Hard wired control unit for accumulator based architecture.

(b) Implement a multiplier control unit, take multiplier of your choice.

(c) Draw the basic structure of microprogrammed control unit and explain its working.

5. Attempt any **two** parts of the following : **(2×10=20)**

(a) Differentiate between look aside and look through type organization of Caches. Draw the block diagram and explain the working.

(b) What do you mean by address mapping ? List the various stages at which the address mapping takes place. Draw the block diagram of dynamic address translation system and explain it.

(c) Discuss the architecture of 8085. Explain its any two applications.