**Printed Pages : 2**                                                            **EEC402**

(Following Paper ID and Roll No. to be filled in your Answer Book)

**PAPER ID : 0322**          Roll No. ☐☐☐☐☐☐☐☐☐☐

## B.Tech.
### (SEMESTER. IV) THEORY EXAMINATION, 2012-13
### COMPUTER ARCHITECTURE & ORGANIZATION

*Time : 3 Hours ]*                                              *[ Total Marks : 100*

### SECTION – A

$10 \times 2 = 20$

1.    Attempt **all** parts of this question :

   (a)    What is design methodology ?

   (b)    Name the different design levels of computer design.

   (c)    Draw the block diagram of processor-memory communication.

   (d)    What is Normalization and Biasing ?

   (e)    What is fixed point arithmetic ?

   (f)    Write down the general formulas for floating-point operations.

   (g)    What do you mean by Control Path of a design ?

   (h)    What do you mean by effective address of data ?

   (i)    What are Horizontal and Vertical micro-instructions ?

   (j)    What is Multiprogramming & Pipe Lining ?

### SECTION – B

2.    Attempt any **three** parts of this question :                    $3 \times 10 = 30$

   (a)    What is register level design ? Design a single function circuit performing $Z: = A + B$ and a multifunction circuit for the same.

   (b)    Discuss Architectural Extensions in which basic design of small accumulator-based CPU can be improved. Draw the organization of processor with foregoing features.

   (c)    What are Combinational Array Multipliers ? Illustrate the Booth multiplication Algorithm.

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(d) List the major steps of the classical design method for control path. Design a All-NAND classical design for the control unit of the gcd processor.

(e) Explain control unit organization. Differentiate between spatial and temporal locality of reference. Aid your answer with suitable examples.

## SECTION – C

Attempt **all** questions & Attempt any **two** parts from each question :                    $5 \times 10 = 50$

3. (a) Explain Internal organization of a CPU and Cache Memory.

   (b) Discuss about advantages and disadvantages of PLD's.

   (c) Design a 4-bit register with parallel I/O and 4-bit register with parallel load.

4. (a) What is the need of addressing mode ? A two word instruction is stored in memory at an address designated by symbol W. The address field of the instruction (stored at W + 1) is designated by symbol Y. The operand used during the execution of instruction is stored at an address symbolized by Z.

   An index register contains the value X. Show how Z is calculated from other address if the addressing mode of the instruction is (i) direct (ii) indirect.

   (b) Discuss about Exceptional conditions in arithmetic operations involving n-bit numbers.

   (c) Explain with block diagram Error Detection and Correction Logic.

5. (a) What are high speed adders ? Design a Carry Lookahead adder.

   (b) Design a data path unit with an ALU and a register file.

   (c) Draw and explain data path of a floating-point arithmetic unit.

6. (a) Draw a structure of an 8M x 8 bit DRAM chip. Explain its specifications.

   (b) Draw a structure of a translation look-aside buffer and explain its working.

   (c) Explain the organization of a four stage instruction pipelining.

7. (a) Draw and explain typical micro programmed controller.

   (b) What is program control unit ? Design a state transition graph for the accumulator – based CPU.

   (c) Describe through diagram how matched word can be read out from an associative memory.

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