

(Following Paper ID and Roll No. to be filled in your Answer Book)

**PAPER ID : 0322**

Roll No.

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**B. Tech.**

(SEM. IV)-THEORY EXAMINATION 2010-11

**COMPUTER ARCHITECTURE AND ORGANIZATION**

*Time : 3 Hours*

*Total Marks . 100*

**Note :** Attempt all questions. All questions carry equal marks.

1. Attempt any **four** parts of the following : (5×4=20)
  - (a) Explain the difference between structure and behaviour in the digital system context.
  - (b) What do you understand by design levels in the design of computer system ? Explain in brief.
  - (c) Discuss the general approach to the design problem for register level system.
  - (d) Explain the various design aspects of processor level design.
  - (e) Draw the block diagram of a dual 4 to 1 line multiplexers and explain its operation by means of a function table.
  - (f) Design a pipelined 4 bit stream serial adder at register level.
  
2. Attempt any **four** parts of the following : (5×4=20)
  - (a) What do you mean by pipelining ? Explain instruction pipelining with the help of example.

- (b) Explain the concept of stack organization.
- (c) What is normalized number according to IEEE ? How are they represented ?
- (d) What do you understand by addressing modes ? Discuss the various types of addressing modes.
- (e) List the criteria for using macros instead of subroutines to structure assembly language program.
- (f) Write a program to evaluate the arithmetic statement

$$X = (A + B) \times (C \times D)$$

Use an accumulator type computer with one address instruction.

3. Attempt any **two** parts of the following : **(10×2=20)**

- (a) Describe the design of a 4-bit carry look ahead adder.
- (b) Explain how Booth's algorithm is suitable for signed number multiplication. Perform the multiplication of following using Booth algorithm  $-4 \times -5$ .
- (c) (i) Explain the floating point multiplication with the help of flowchart.
- (ii) List the advantages and disadvantages of designing a floating point processor in the form of K-stage pipeline.

4. Attempt any **two** parts of the following: **(10×2=20)**

- (a) Explain the difference between hardwired control and micro-programmed control. Is it possible to have a hardwired control associated with a control memory ? Also define the following terms :

- (i) Microoperation
  - (ii) Microinstruction
  - (iii) Microcode
  - (iv) Microprogram.
- (b) Give the block diagram of microprogram sequencer for a control memory and explain it properly.
- (c) What do you understand by term Superscalar ? Explain the concept of superscalar processing.
5. Attempt any **two** parts of the following : **(10×2=20)**
- (a) What is Cache Memory ? How is it implemented ? A two way set associated cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K ×32.
- (i) Formulate all pertinent information required to construct the cache memory.
  - (ii) What is the size of cache memory ?
- (b) Explain the Daisy chaining mechanism for bus arbitration. Analyze the three bus arbitration methods–Daisy chaining, polling and independent requesting with respect to communication reliability in the event of hardware failures.
- (c) Draw and discuss the internal architecture of 8085.