

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3072

Roll No.

|  |  |  |  |  |  |  |  |  |  |
|--|--|--|--|--|--|--|--|--|--|
|  |  |  |  |  |  |  |  |  |  |
|--|--|--|--|--|--|--|--|--|--|

**B.Tech.****(SEM. III) ODD SEMESTER THEORY****EXAMINATION 2013-14****SWITCHING THEORY****Time : 3 Hours****Total Marks : 100****Note :—Attempt all questions.****1. Attempt any four :****(4×5=20)****(a) Perform the following operation :****(i)  $(1011)_2 - (0100)_2$  using 1's complement method****(ii)  $(4)_{10} - (9)_{10}$  using 2's complement method****(iii) Add  $(569)_{10}$  and  $(687)_{10}$  in BCD.****(iv) Obtain the XS - 3 code for  $(428)_{10}$** **(v) Encode the decimal number 46 to gray code.****(b) A bit word 1011 is to be transmitted. Construct the even parity seven bit Hamming code for the data.****(c) Write a short note about error detection and correction codes. Describe the cyclic codes.****(d) Simplify the following logic expression :****(i)  $Y = \pi M(1, 3, 5)$** **(ii)  $Y = \Sigma M(2, 4, 6)$** **(e) Minimize the following expression using the K-map :**

$$Y = \Sigma m(1, 5, 6, 7, 11, 12)$$

**(f) Distinguish between static and dynamic hazard.**

2. Attempt any two : (2×10=20)

- (a) Explain the block diagram of a combinational circuit. Design the full address using half address and verify its truth table.
- (b) Implement the following boolean function using all 4:1 multiplexers :

$$F(A, B, C, D, E) = \sum m(0, 1, 2, 3, 6, 8, 9, 10, 13, 15, 17, 20, 24).$$

- (c) Give the comparison of PROM, PLA and PAL.

A combinational logic is defined by function-

$$F_1(A, B, C) = \sum m(3, 5, 6, 7)$$

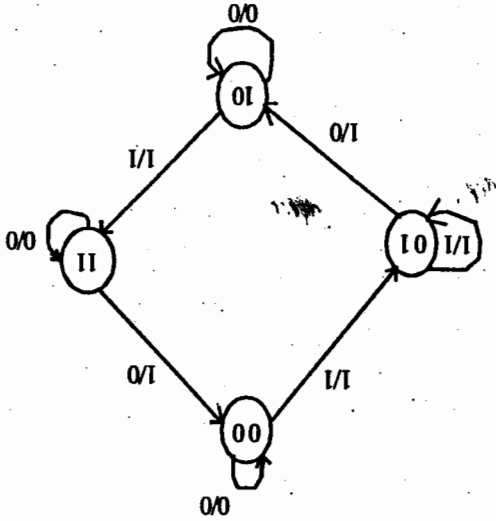
$$F_2(A, B, C) = \sum m(0, 2, 4, 7)$$

Implement the circuit with PLA having 3 input, 4 product term and two output.

3. Attempt any two : (2×10=20)

- (a) Differentiate between latches and flip flop. Design one input and one output D flip flop and draw the circuit for converting it into SR flip flop.
- (b) Distinguish between synchronous and Asynchronous digital sequential circuit. Explain using example circuit of 3 bit binary counter.

- (c) For the following state diagram obtain state table, excitation table and design the circuit using J-K flip flop.

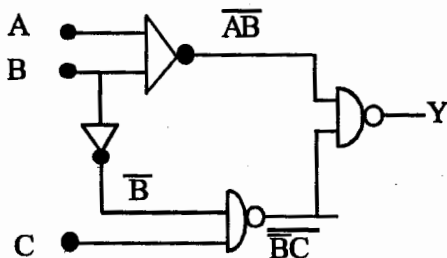


4. Attempt any two : (2×10=20)
- (a) Enlist the basic components of bipolar and unipolar logic family. Explain the various parameters of RTL logic.
- (b) Explain why the temperature sensitivity of HTL is significantly better than DTL. Compare the two with the help of a 3 input NAND gate circuit.
- (c) Draw the interfacing circuit of CMOS and TTL and explain a TTL driving CMOS and a CMOS TTL. Find the fan out when a CMOS driving TTL series gates.

5. Attempt any four :

(4×5=20)

- (a) Distinguish between static and dynamic hazard.
- (b) For the network shown in following diagram, write the transient disjunctive normal formula.



- (c) Classify and characterize the various types of memories.
- (d) Draw a dynamic CMOS shift register for one stage and draw its block diagram. Explain the operation.
- (e) Draw the diagram of a 16-bit ROM-array.
- (f) Explain the various types of ROM and how it is programmed.