Printed Pages : 4 TEC-302

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3072 Roll No.

# B. Tech.

## (SEM. III) EXAMINATION, 2008-09

## SWITCHING THEORY

*Time : 3 Hours]* *[Total Marks : 100*

*Note :* *(i) All questions carry* ***equal*** *marks.*

*(ii) All questions are* ***compulsory.***

1 Attempt any **four** of the following : 5×4=20

(a) How many bits of memory are required for storing **100** names of a group of people, assuming that no name occupies more than **20** characters (including space) ? Assume **7**-bit ASCII code with parity bit.

(b) Encode the decimal number **46** to Gray code.

(c) Determine Hamming code sequence with odd parity for natural BCD for making it an error correcting code.

(d) Realize a **3**-input gate using **2**-input gates for the following gates :

(i) AND (ii) OR (iii) NAND (iv) NOR.

(e) Consider the expression :

$$Z = A \oplus B \oplus C \oplus D \oplus \ldots .$$

Show that $Z = 1$ if an odd number of variables are **1** and $Z = 0$ if an even number of variables are **1**.

(f) Realize the following function using *EX-OR* and *EX-NOR* gates ?

$$f = AB\bar{C}\bar{D} + A\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}BC\bar{D}.$$

2 Attempt any **four** parts of the following : 5×4=20

(a) Design a parity generator to generate even parity bit for a **4** bit word. Use *EX-OR* and $\overline{EX-OR}$ gate.

(b) Design a *BCD* to Excess-**3** code converter using minimum number of NAND gates.

(c) Implement the following function using a **4**-to-**16** line decoder :

$$f = \sum m(1, 2, 4, 7, 8, 11, 12, 13).$$

(d) Present an algorithm for performing subtraction using adder.

(e) Implement the expression using a multiplexer

$$f(A,B,C,D) = \sum m(0,2,3,6,8,9,12,14).$$

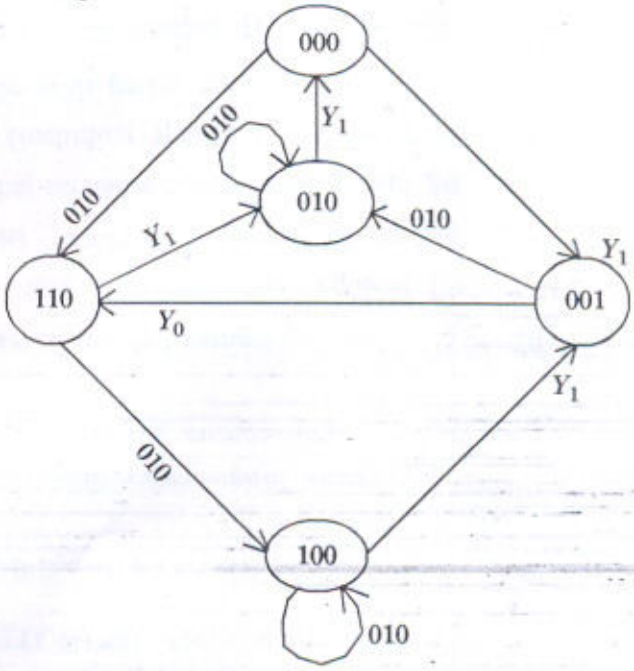
(f) Design a *BCD*-to-seven segment decoder using a PAL.

3 Attempt any **two** of the following : 10×2=20

(a) Describe and discuss the operation of a T-type flipflop.

(b) Design a **3**-bit binary UP/DOWN counter with a direction control *M*, using J-K flip-flops.

(c) Design a circuit using J-K ffs for the state diagram.




4 Attempt any **two** of the following : 10×2=20

(a) Draw and explain "an output circuit arrangement" for explaining "Totem-pole" output for TTL gates.

(b) Distinguish between static and dynamic hazard. How will you determine hazard in combinational circuits ?

(c) Explain the operation of wired-OR connections of ECL gates ?

5 Attempt any **two** of the following : **10×2=20**

(a) Obtain a 16 × 8 memory using 16 × 4 memory ICs and draw the concerned IC circuit.

(b) Explain : Coincident selection addressing.

(c) Draw the circuit for Bipolar RAM cell and explain its operation, in brief.