(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3072 Roll No. | | | | | | | | | | |

B.Tech.

THIRD SEMESTER EXAMINATION, 2006-07

SWITCHING THEORY

Time : 3 Hours *Total Marks : 100*

Note : *(i) Attempt ALL questions.*

(ii) All questions carry equal marks.

(iii) In case of numerical problems assume data wherever not provided.

(iv) Be precise in your answer.

1. Attempt ***any four*** parts of the following : (5x4=20)

(a) Convert the base-7 number $(3\ 5\ 6\ 1\ 4)_7$ to base-12.

(b) Simplify the following Boolean expression which represent the output of a logical decision circuit :

$$f(A, B, C, D) = (AB + C + D)(\overline{C} + D)(\overline{C} + D + E)$$

(c) Perform the following arithmetic operations in BCD numbers :

(i) $954 + 463$

(ii) $893 - 647$

(d) Minimize the following function by Tabular method :

$f(w, x, y, z) = \Sigma m(1, 4, 8, 9, 13, 14, 15) + d(2, 3, 11, 12)$

(e) Determine minimal sum of product form for the following multiple output system (using K-map or Tabular method) :

$f(A, B, C, D, E) = \Sigma m(0, 1, 2, 3, 6, 7, 14, 15, 17, 19, 31)$

(f) Write notes on Hamming code.

2. Attempt *any four* parts of the following : **(5x4=20)**

(a) What are the different types of parallel adders ? Explain carry save and carry look-ahead adders.

(b) Using four-input multiplexers, implement the following functions :

(i) $f(A, B, C) = \Sigma m(0, 2, 3, 5, 7)$ control variables A and B.

(ii) $f(A, B, C) = \Sigma m(1, 3, 4, 6, 7)$ control variables B and C.

(c) Design a code converter that converts a decimal digit from the 8 - 4 - 2 - 1 code.

(d) How will you use ROM as decoder ? Justify your answer.

(e) Design a two digit BCD adder with the help of 4-bit binary adders.

(f) Explain the following :

(i) Amplitude comparator

(ii) PLA

3. Attempt *any two* parts of the following : **(10x2=20)**

(a) Describe the following in brief :

(i) Excitation table and next state equation of FFs.

(ii) Design of sequential circuits using flow-chart.

(b) Design a synchronous counter using J-K flip-flops for the following input sequences :

A	B	C
0	0	0
1	0	1
1	1	0
1	1	1
0	1	1
0	1	0
0	0	0

this repeats

(c) Answer the following :

(i) What are the steps for the analysis of asynchronous sequential circuit ?

(ii) Define ASM action blocks.

(iii) How do you convert the state diagram to ASM chart ?

4. Attempt *any two* parts of the following : **(10x2=20)**

(a) What is meant by open collector output of TTL gate ? What is its utility ? Draw the circuit showing open collector output and pull-up resistor. Explain its operation.

What are the applications of open collector output ?

(b) What are the advantages of BiCMOS logic circuits ? Draw the circuits of BiCMOS NAND and NOR gates. Explain their operations.

Draw a circuit diagram to interface CMOS to TTL.

(c) Answer the following :

(i) Write merits/demerits of different logic families.

(ii) Explain the parameters used to characterize logic families.

(iii) How will you determine NAND gate delay in the laboratory ?

5. Attempt *any two* parts of the following : **(10x2=20)**

(a) Plot K-map of the following functions :

(i) $f(A, B, C, D) = \Sigma m (0, 2, 4, 5, 6, 8, 9, 11, 12, 14, 15)$ and

(ii) $f(A, B, C, D) = \Sigma m (3, 4, 5, 6, 11, 12, 13, 14, 15)$

Determine hazard free implementation in both above cases, using :

(1) NAND gates

(2) NOR gates

It can be assumed that gate having a maximum Fan-in of three.

(b) Develop a fault detection table for the circuit shown in figure 5 (b).

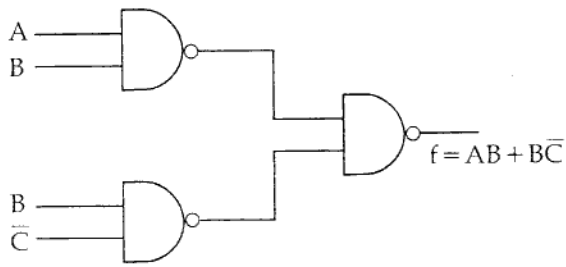

Figure 5 (b)

(c) Write short notes on the following :

(i) Formation of memory banks

(ii) Static and dynamic memories

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