04350

Printed Pages—4

TEC – 302

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3072   Roll No. | | | | | | | | | | |

B.Tech.

THIRD SEMESTER EXAMINATION, 2005-2006

SWITCHING THEORY

Time : 3 Hours   Total Marks : 100

Note : (i)   Answer ALL questions.

(ii)   All questions carry equal marks.

(iii) Be precise in your answer

1. Attempt *any four* of the following questions :   (5×4=20)

(a) Convert the base - 5 number $(4433214)_5$ directly to base - 12.

(b) Simplify the following Boolean expression which represent the output of a logical decision circuit

$$f(w, x, y, z) = x + xyz + \overline{x}\, yz + \overline{w}x + \overline{w}\,x + \overline{x}\,y$$

(c) Perform the following arithmetic operations

(i)   Add 96 and 56 BCD numbers.

(ii) Subtract 748 from 983 BCD number.

(d) Minimize the following function by Tabular method

$$f(A, B, C, D) = \sum m\,(0, 2, 3, 6, 7, 8, 9, 10, 13)$$

TEC – 302   1   [Turn Over

(e) Determine minimal sum of product form for the following multiple output system (Use K - map or Tabular method).

$$f_1 (a,b,c) = \sum m (0,1,3,5)$$

$$f_2 (a,b,c) = \sum m (2,3,5,6)$$

$$f_3 (a,b,c) = \sum m (0,1,6)$$

(f) What is cyclic code ? Write the principle of detection and correction of one-bit error with the help of it.

2. Attempt *any four* of the following questions :   (5x4=20)

(a) Explain with suitable diagram the working principle of 4-bit CLA adder and determine expression for the fourth carry.

(b) Design the following Boolean function using the multiplexer.

$$f (A,B,C,D) = \sum m (0,1,3,4,8,9,15)$$

(c) Explain the priority encoder.

(d) Design one digit BCD adder with the help of 4-bit binary adders.

(e) Draw the circuit of four - bit amplitude comparater and explain its operation.

(f) Explain the following :

(i)   PAL

(ii)   Code - convertors.

3. Attempt *any two* of the following questions : **(10x2=20)**

(a) What are synchronous and asynchronous sequential circuits ? Write the procedure for the analysis of a sequential circuit.

Draw the state diagram for a sequence generator which produces an output '1' every time the sequence 0101 is detected and output '0' at all other times. Design the circuit also.

(b) An asynchronous sequential circuit is described by the following excitation and output functions.
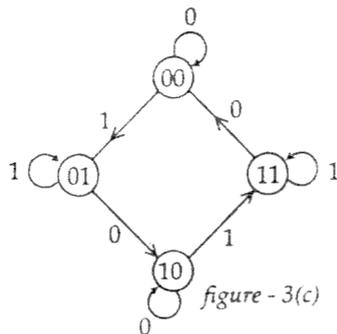
$$y = x_1 x_2 + (x_1 + x_2) y$$
$$z = y$$

Where x_1 & x_2 = input variables

y = excitation function

z = output function

(i) Draw the logic diagram and

(ii) Derive transition table and output-map.

(c) Answer the following :

(i) Explain in brief the ASM chart.

(ii) Draw an equivalent ASM chart of a state diagram shown in figure 3 (c).

figure - 3(c)

(iii) Write the applications of shift registers.

4. Attempt *any two* of the following questions : (10x2=20)

(a) Draw a TTL circuit with totem pole output and explain its working why should it not be used for wired AND connection ? Write the chip number of a two - input quad TTL NOR gate.

(b) What is meant by CMOS and BiCMOS ? Explain the working of CMOS NAND and NOR gates. Draw the circuit diagram to interface TTL to CMOS. Design a 8-bit bidirectional bus using tri-state logic.

(c) Answer the following :

(i) What are the classification of logic family ?

(ii) Explain the terms fan-in, fan-out, propagation delay and power dissipation.

(iii) How will you determine Ex-OR gate delay in the laboratory ?

5. Attempt *any two* parts of the following : (10x2=20)

(a) What is various type of hazard in digital circuits? Explain the terms; Struck at 0 and stuck at 1 faults. Find a circuit that has no static hazards and implements the following Boolean function

$$f(A,B,C,D) = \sum m (0,2,6,7,8,10,12)$$

(b) Explain the various method to detect fault. Develop a fault detection table for the circuit given in figure 5 (b).
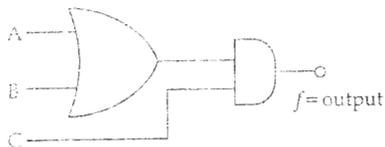

Figure 5 (b)

(c) Write short notes on the following :

(i) Sequential and Random Access memories.

(ii) One and multi-dimensional selection arrangements of memories.

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